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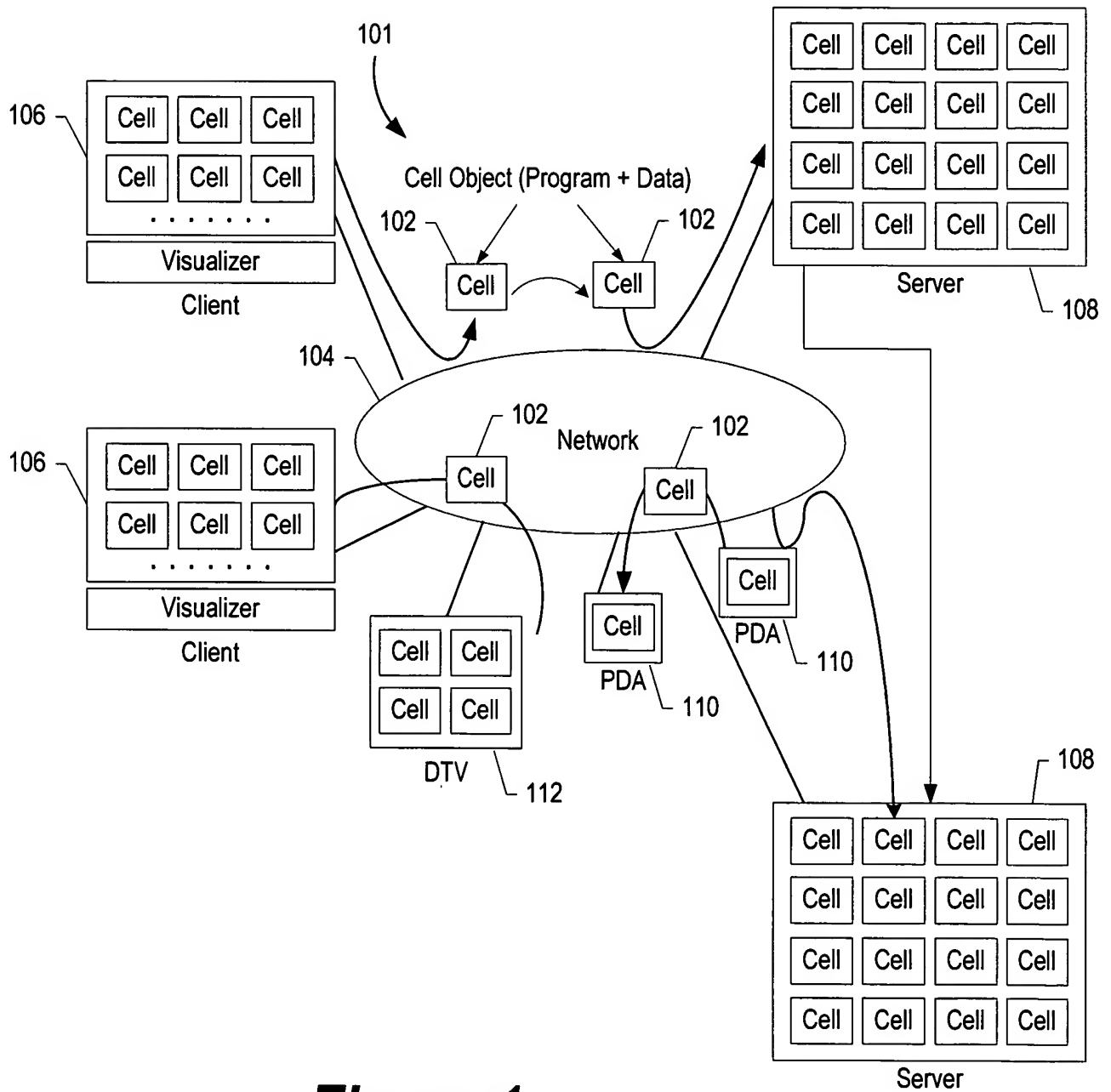
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**Figure 1**

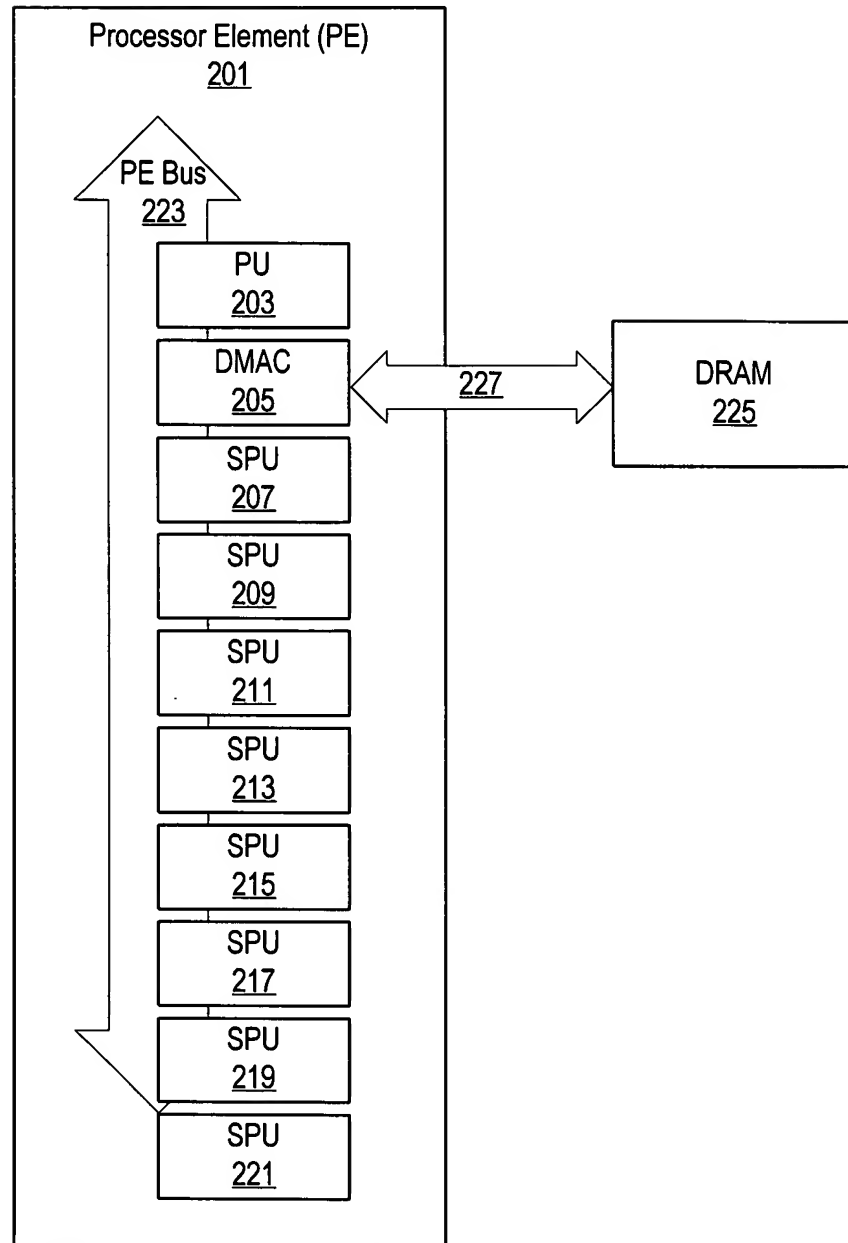


Figure 2

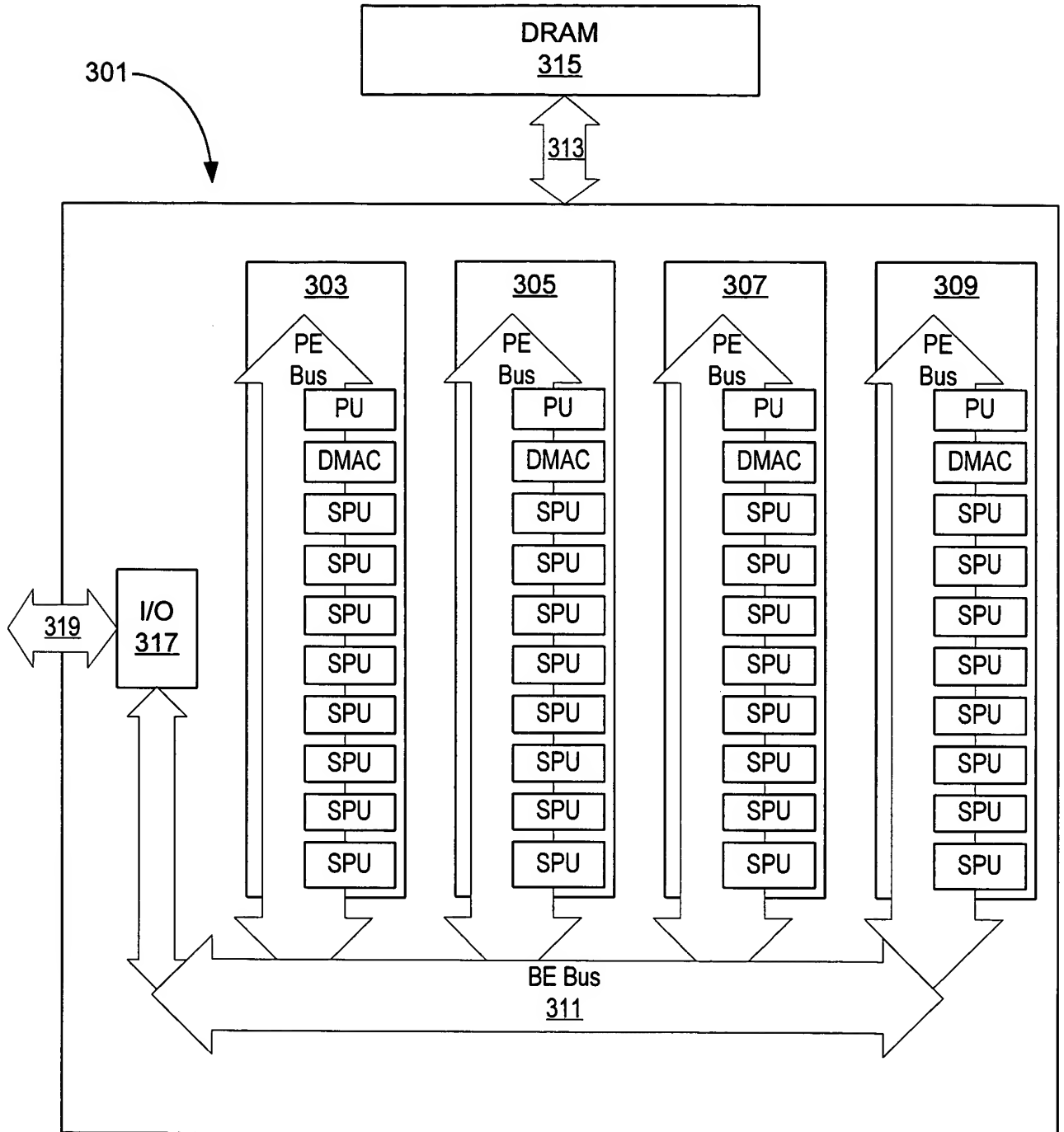


Figure 3

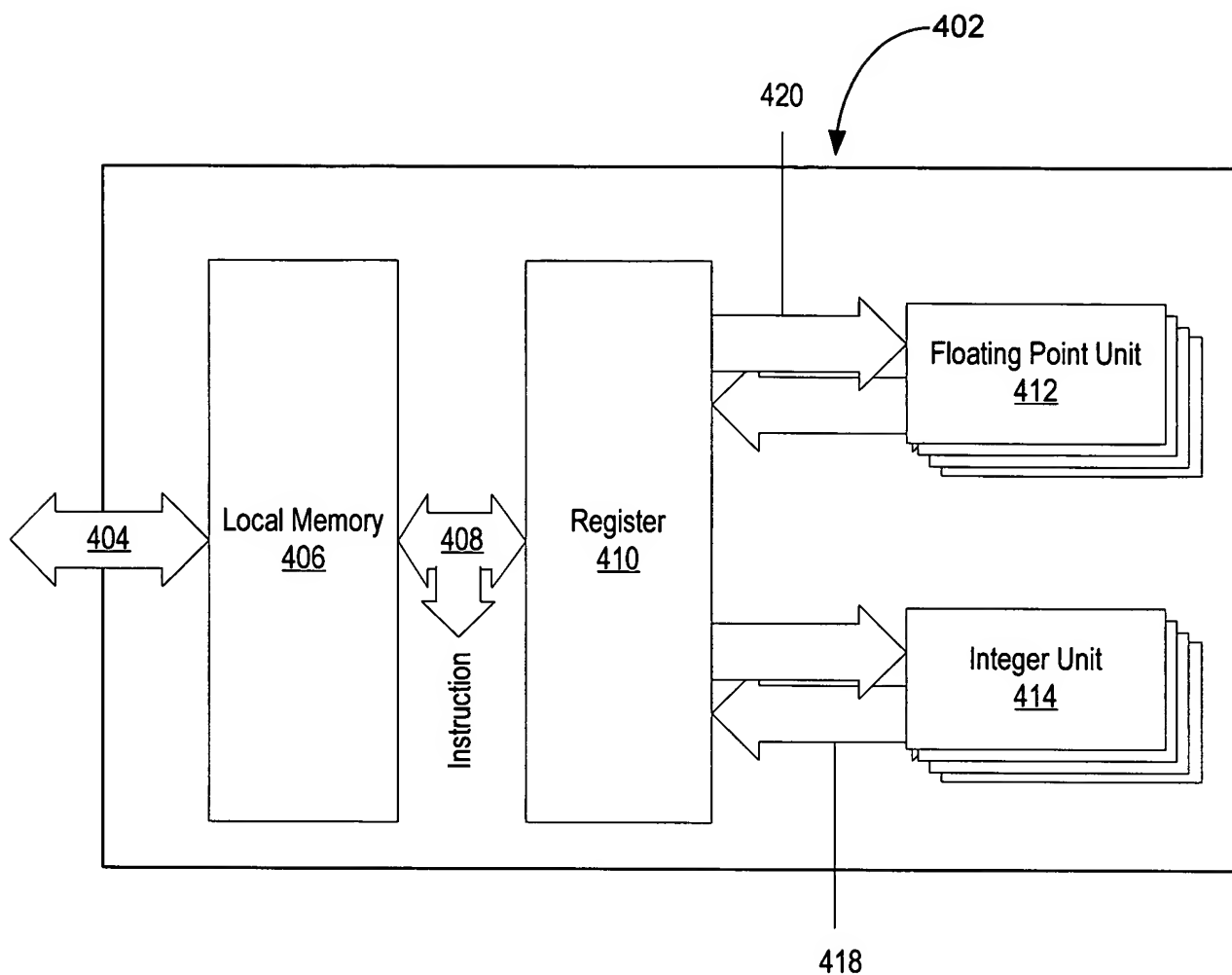


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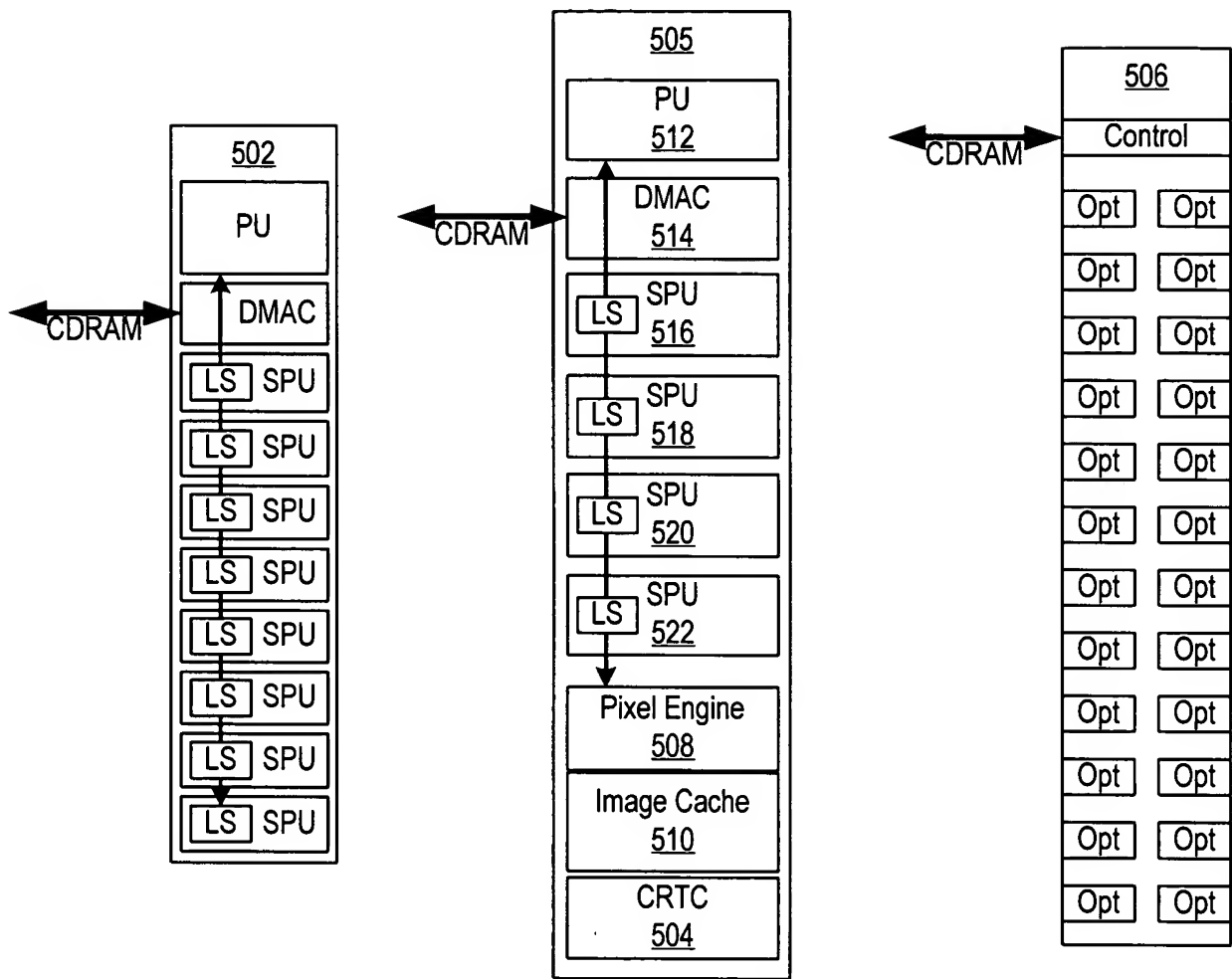


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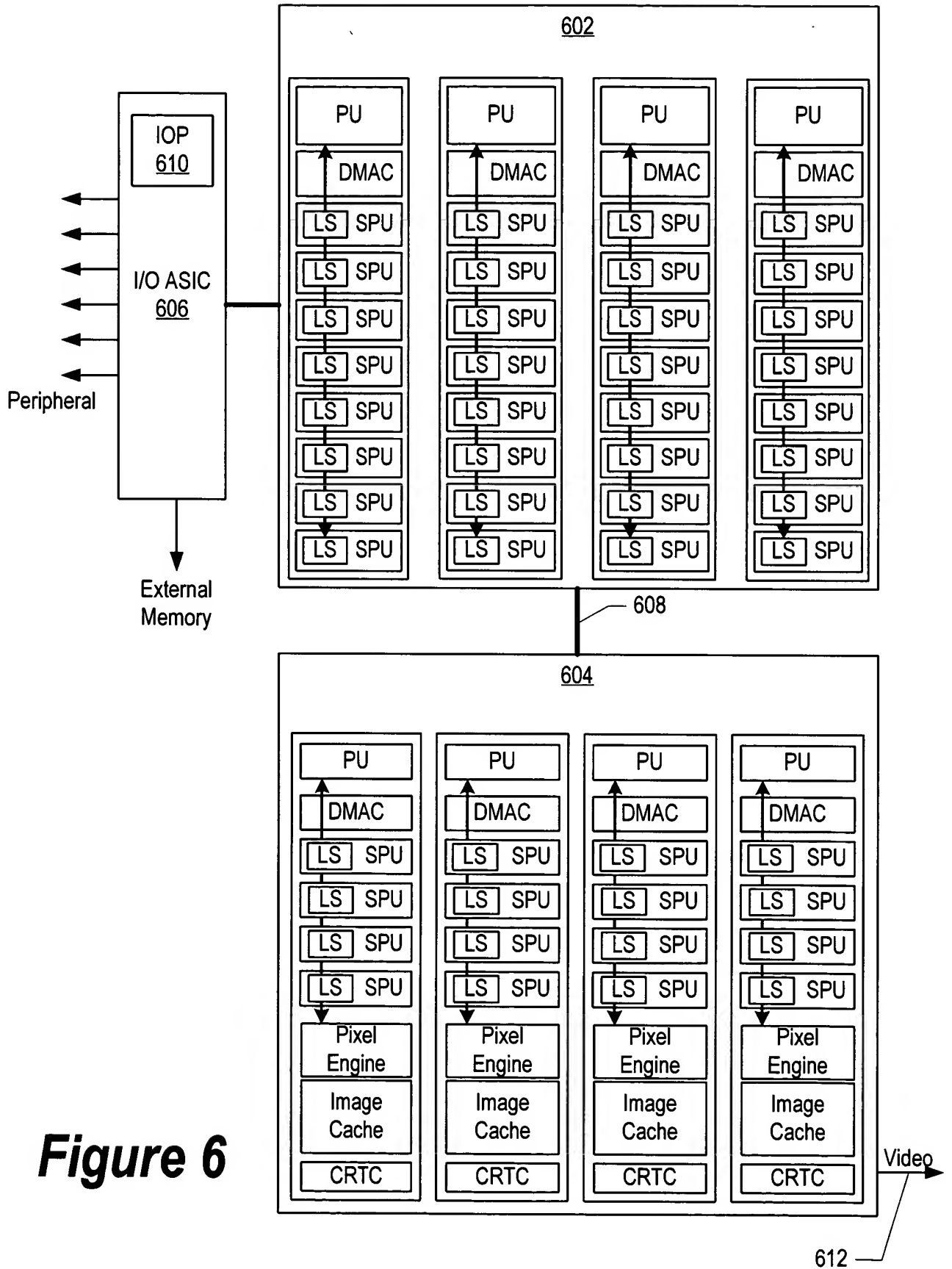


Figure 6



Figure 7

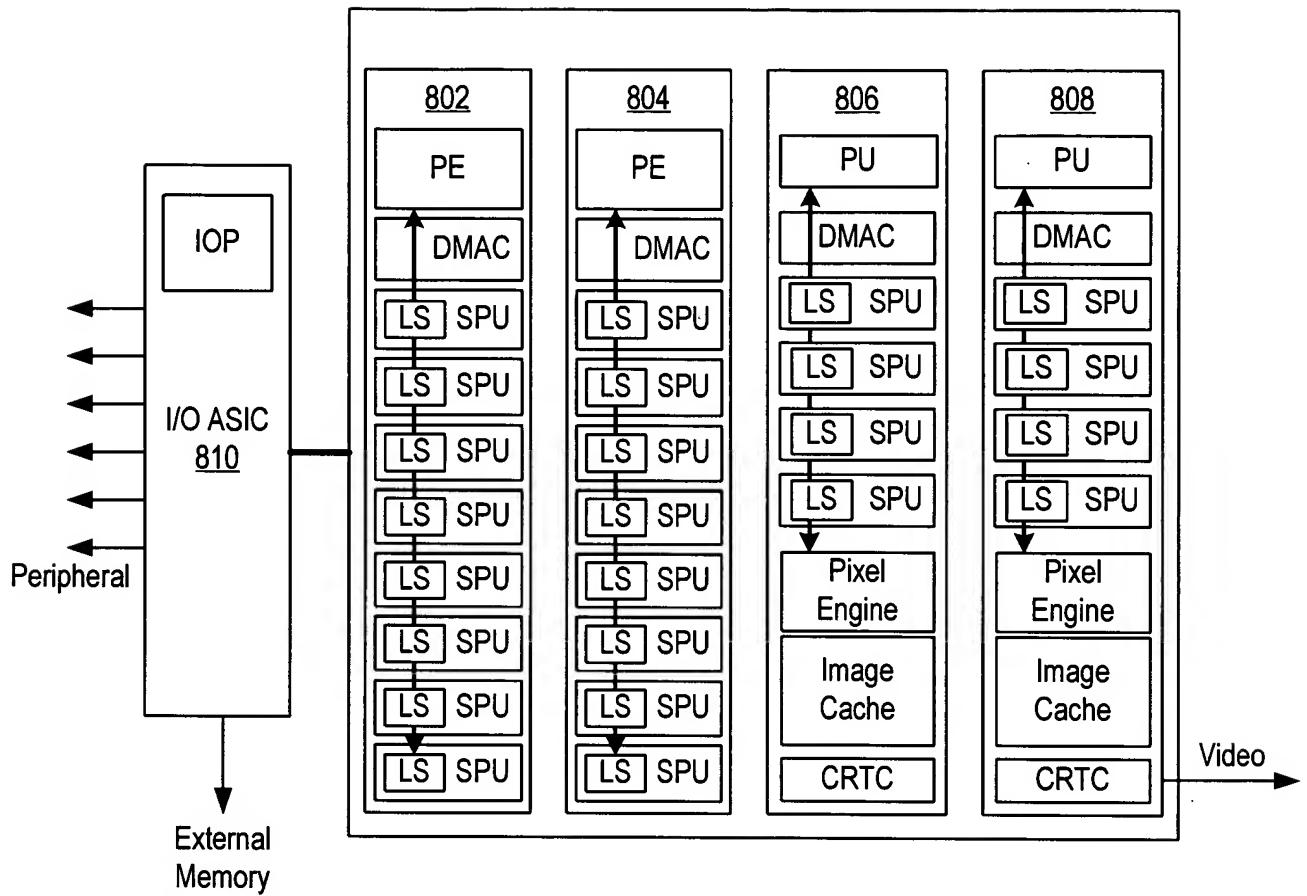


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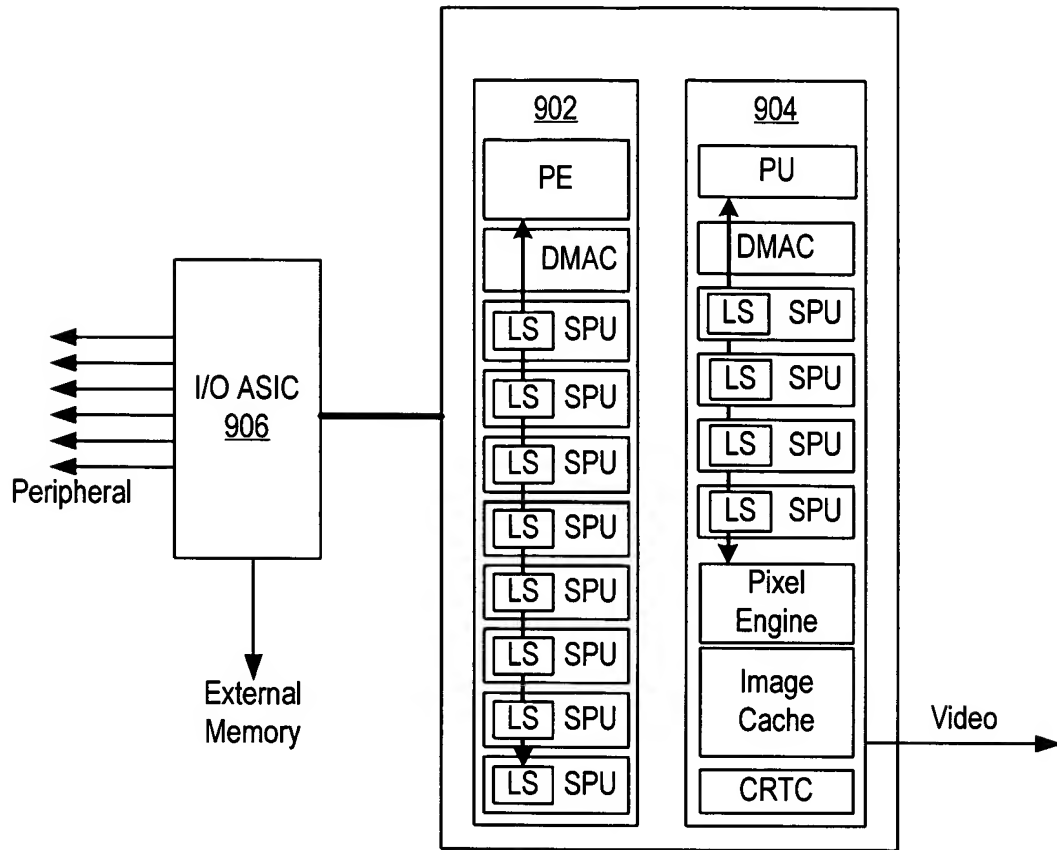


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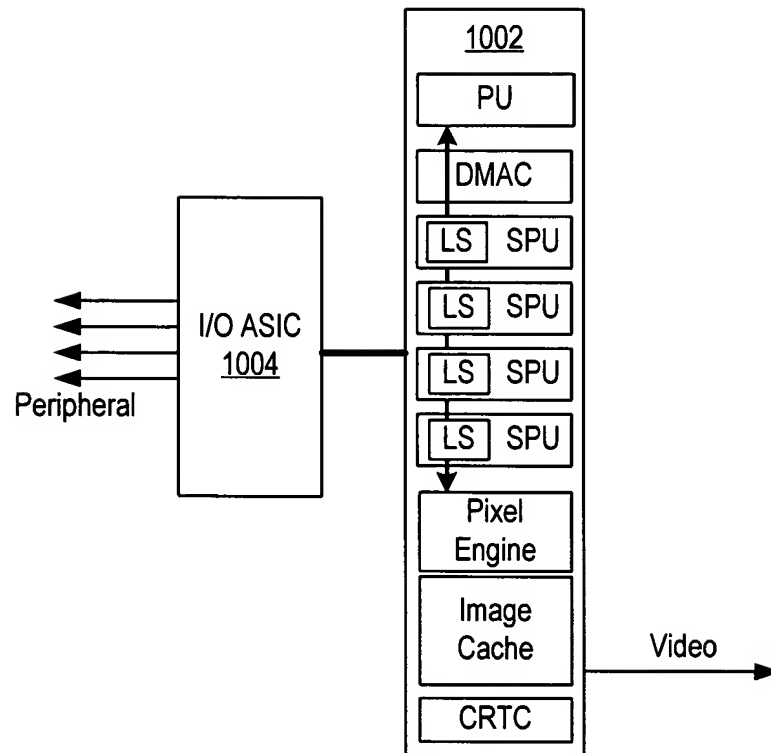


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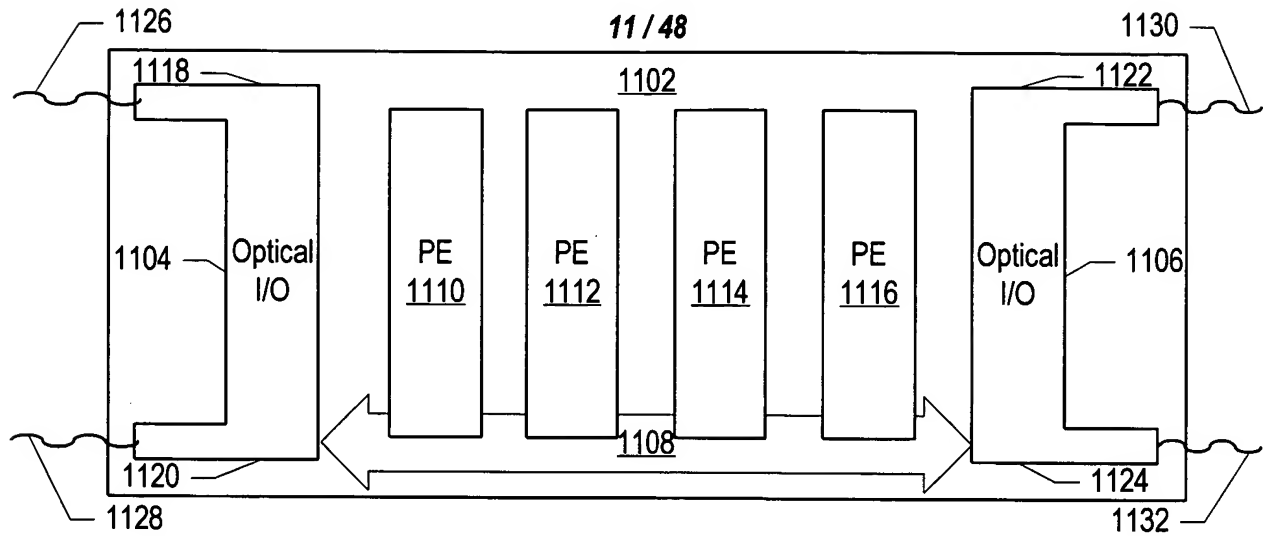


Figure 11A

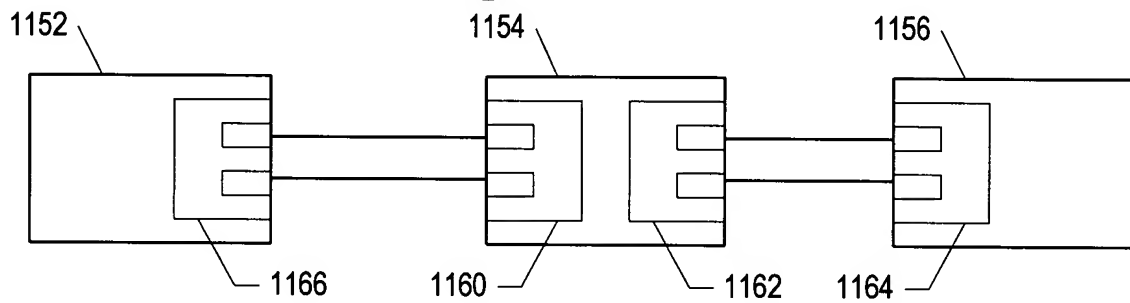


Figure 11B

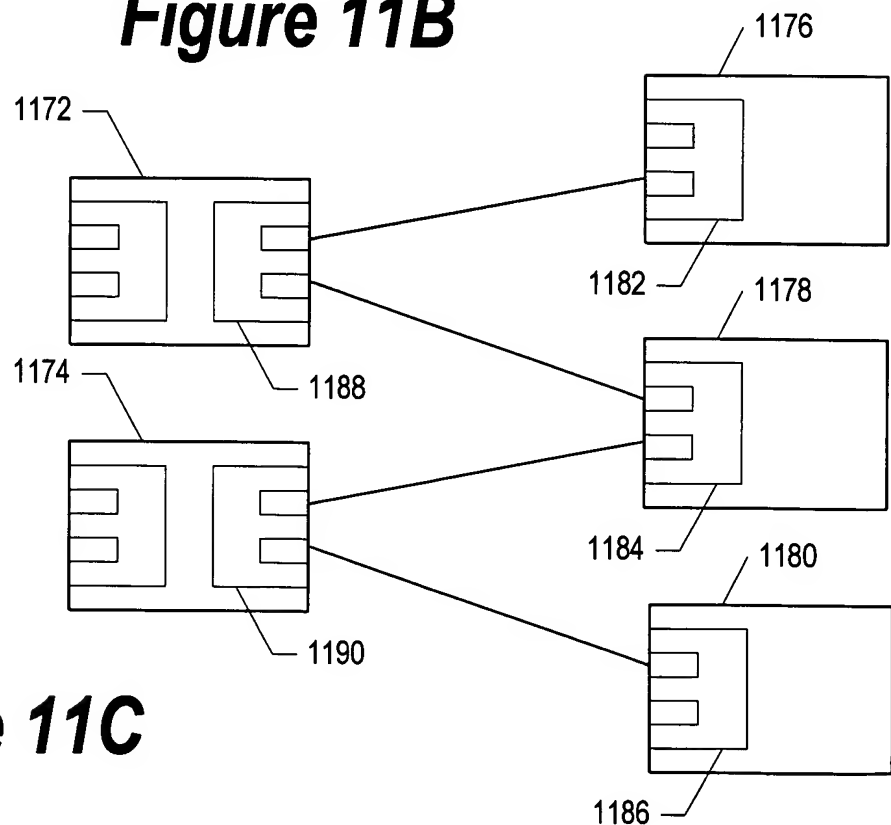
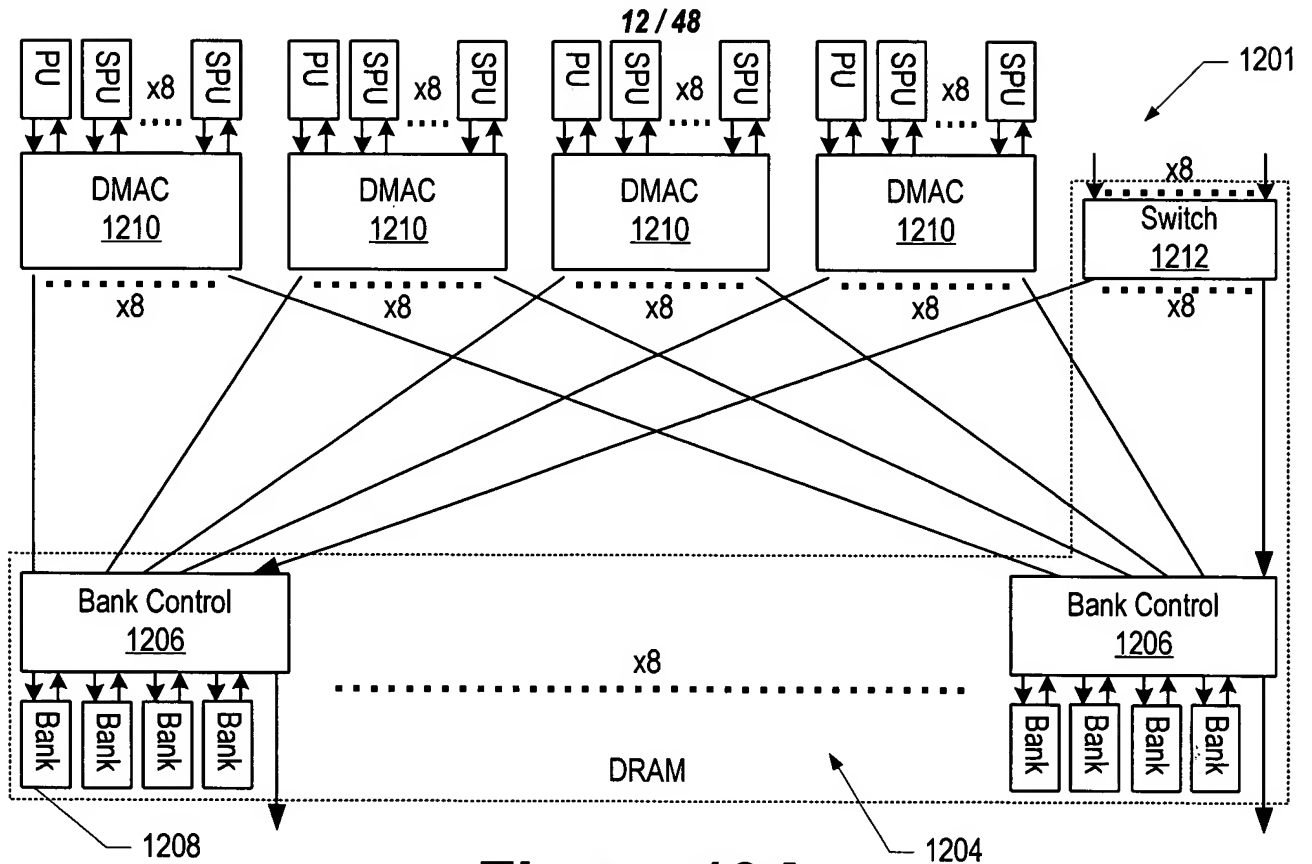
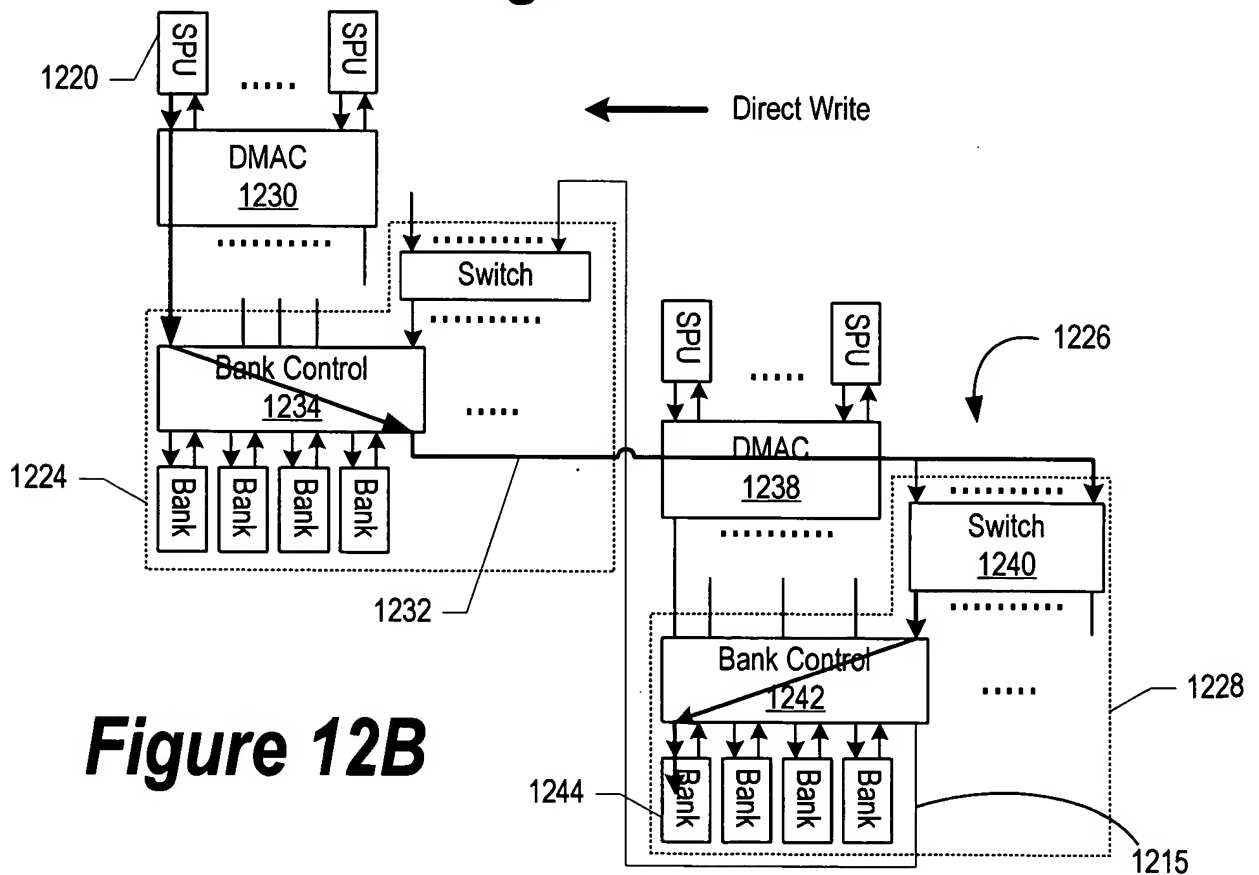


Figure 11C

**Figure 12A****Figure 12B**

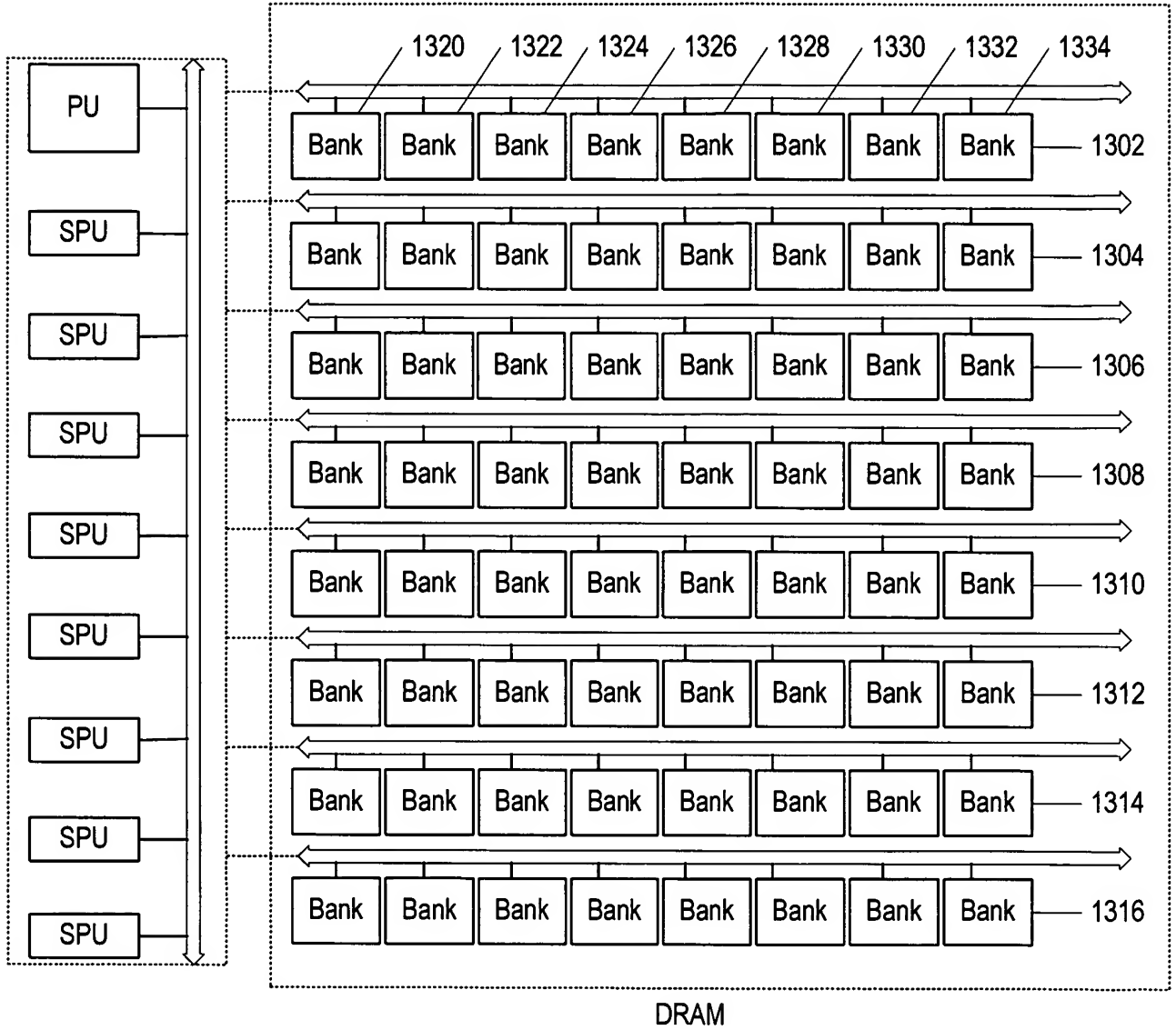


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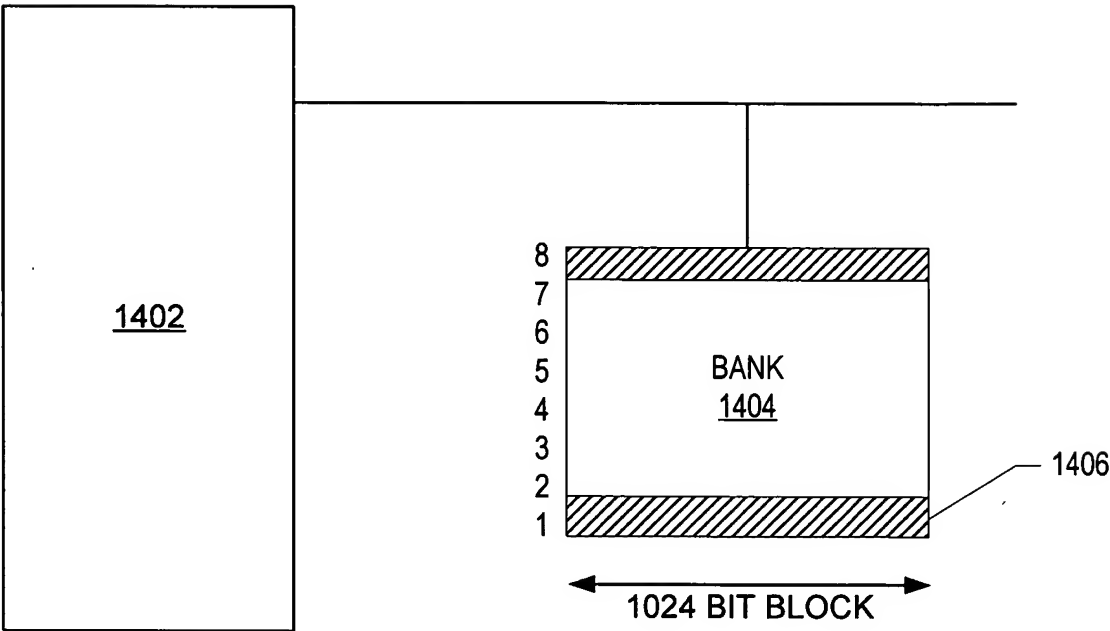


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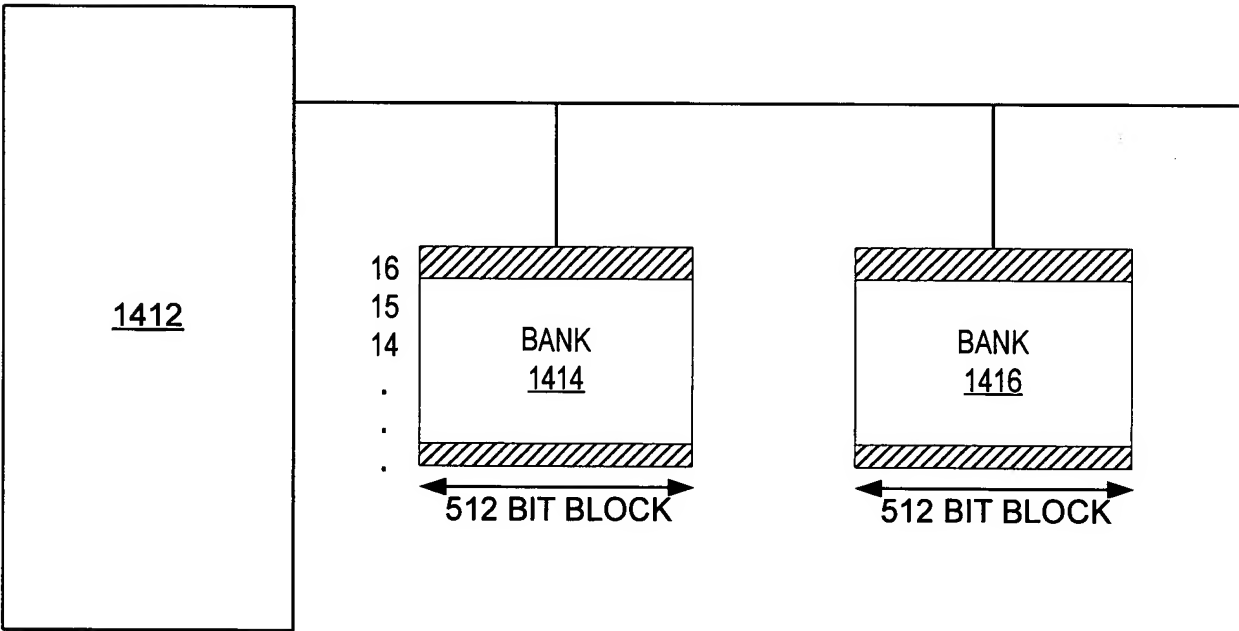


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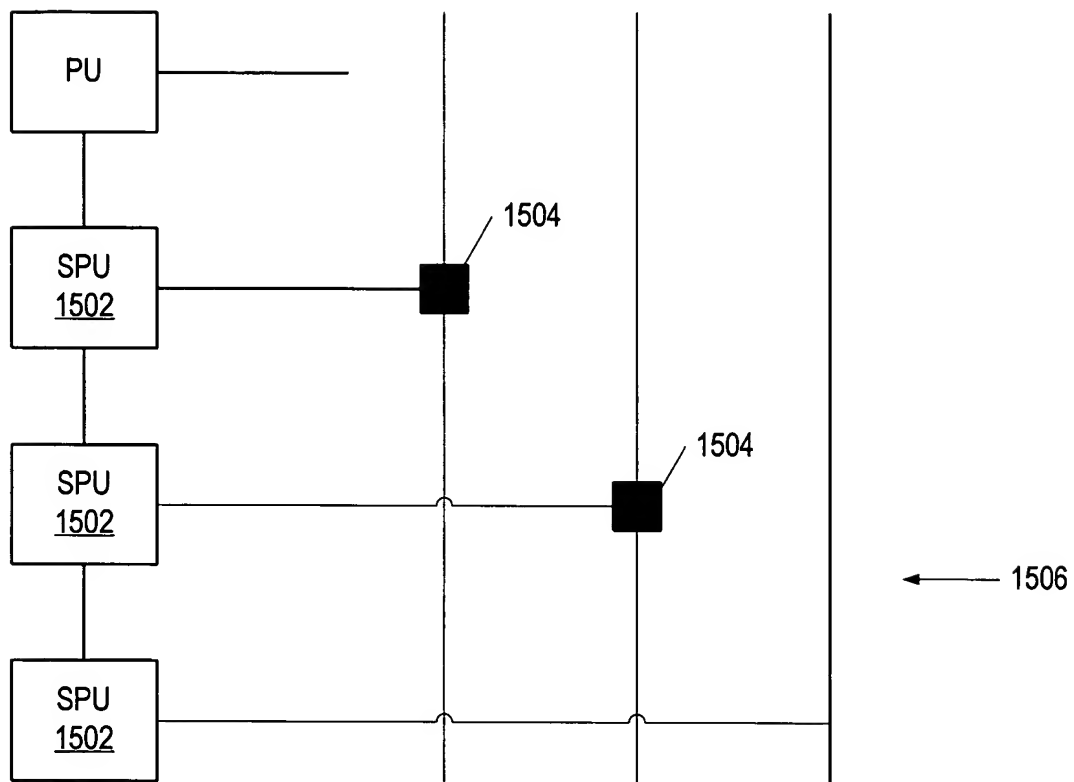


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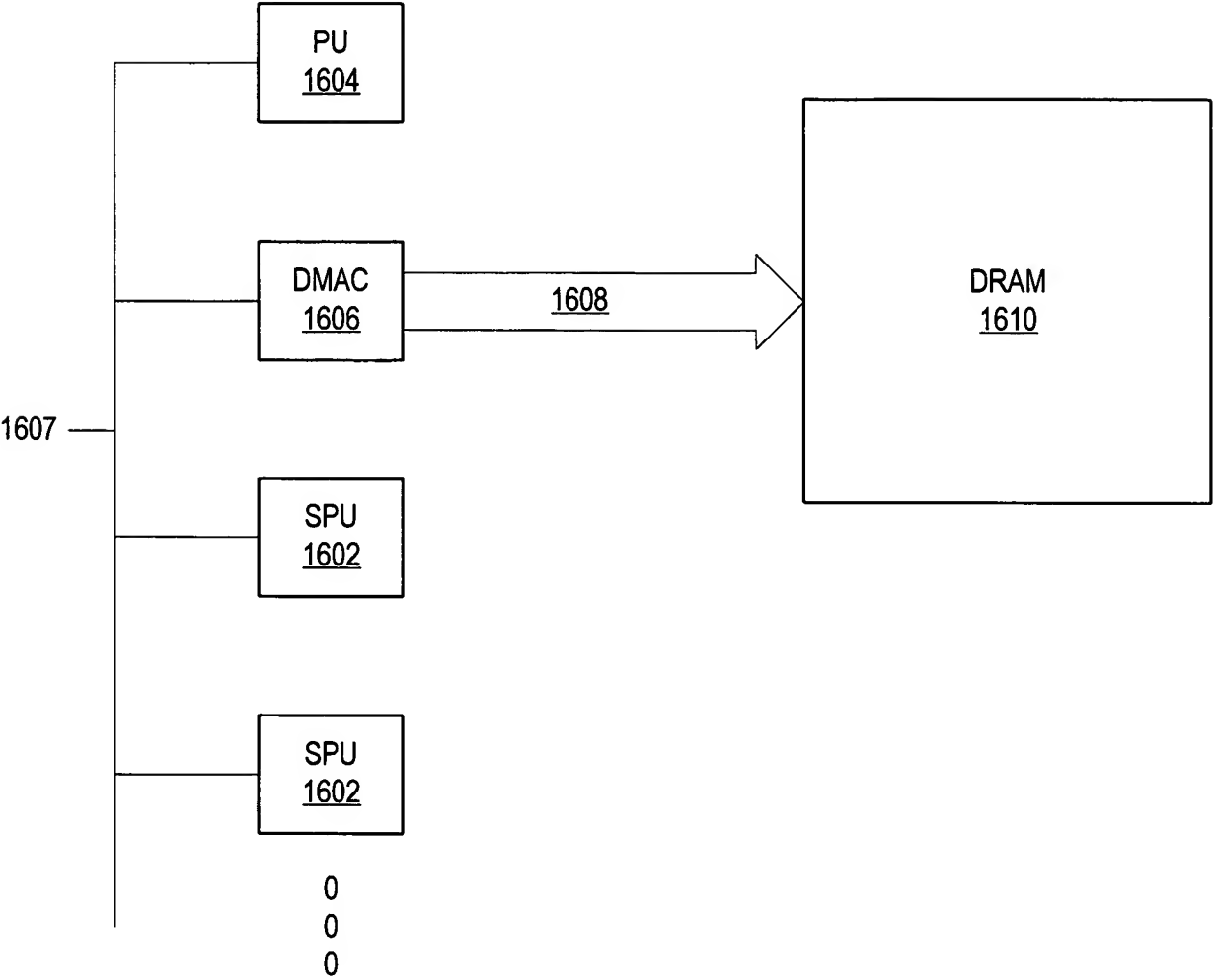


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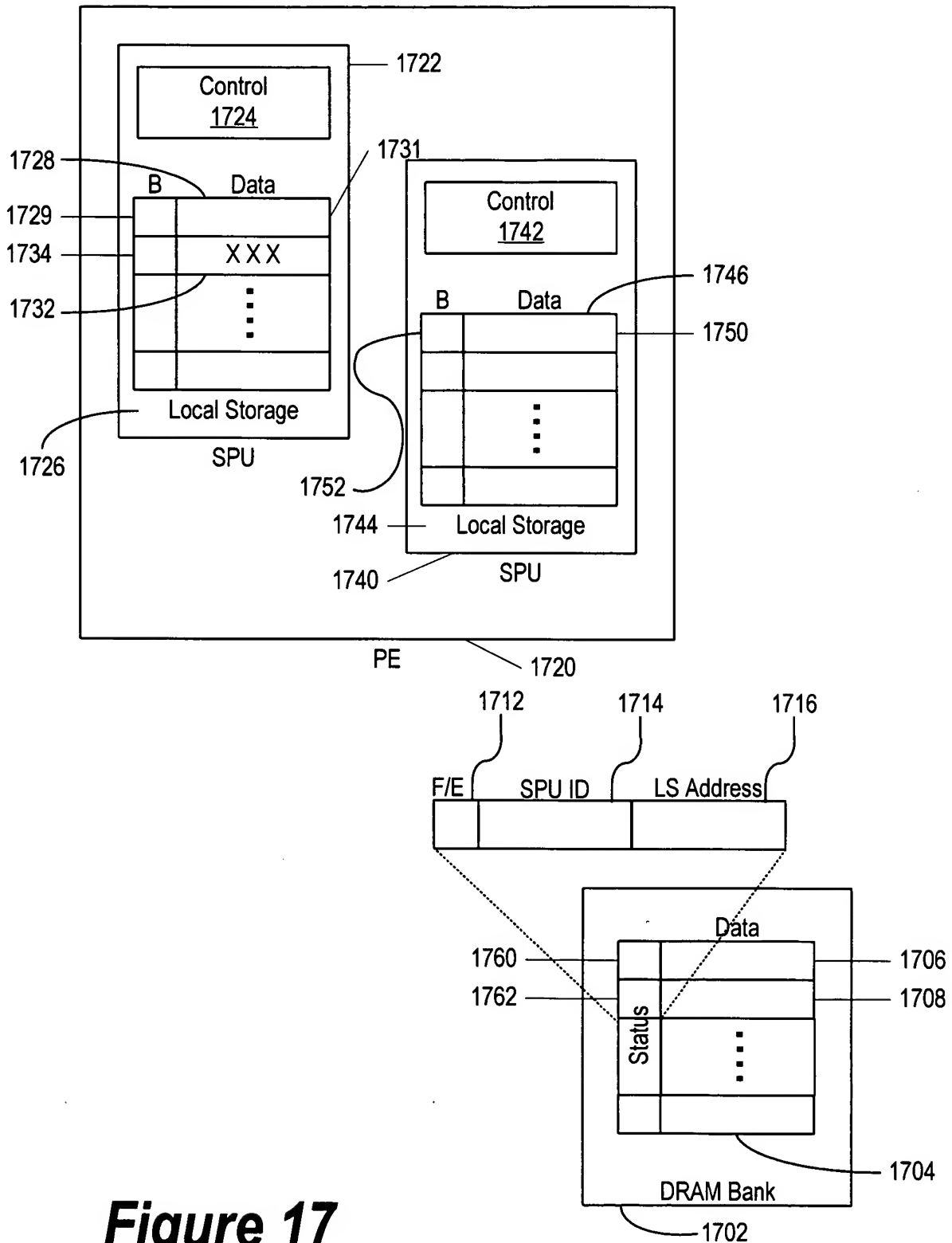


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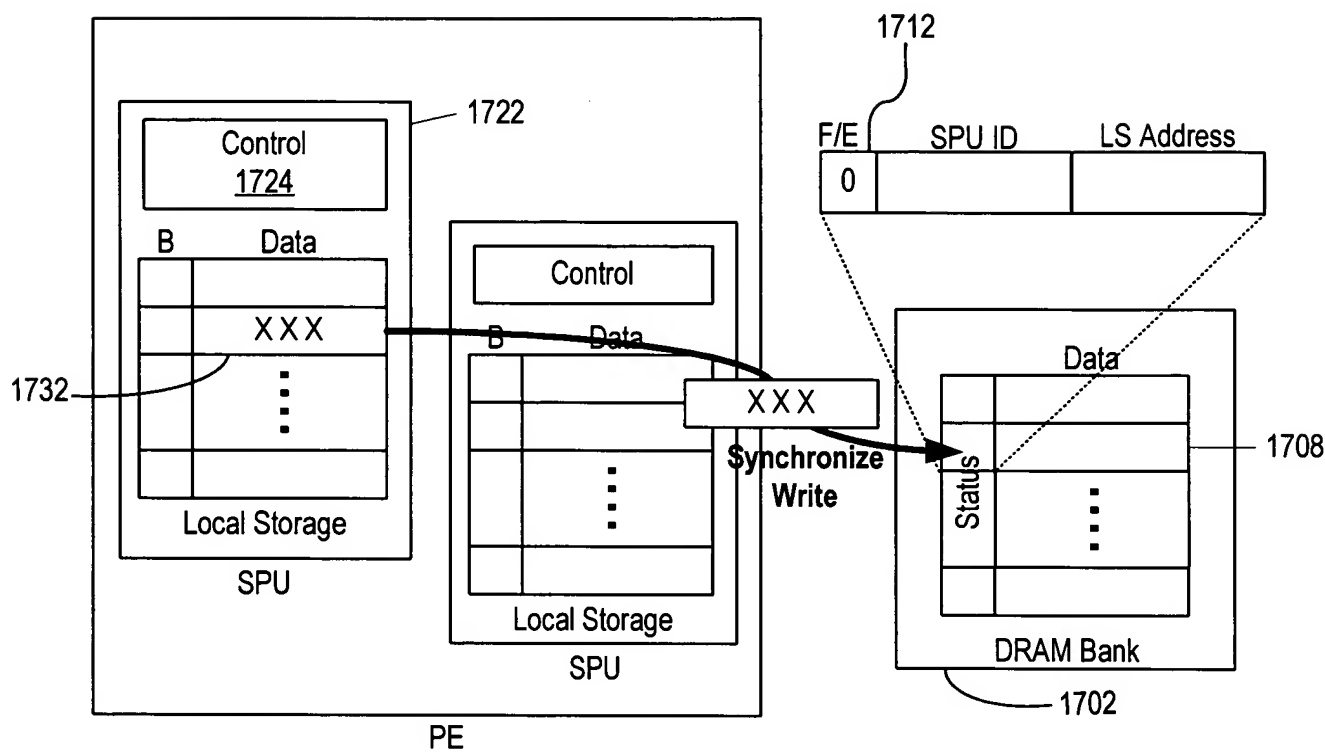


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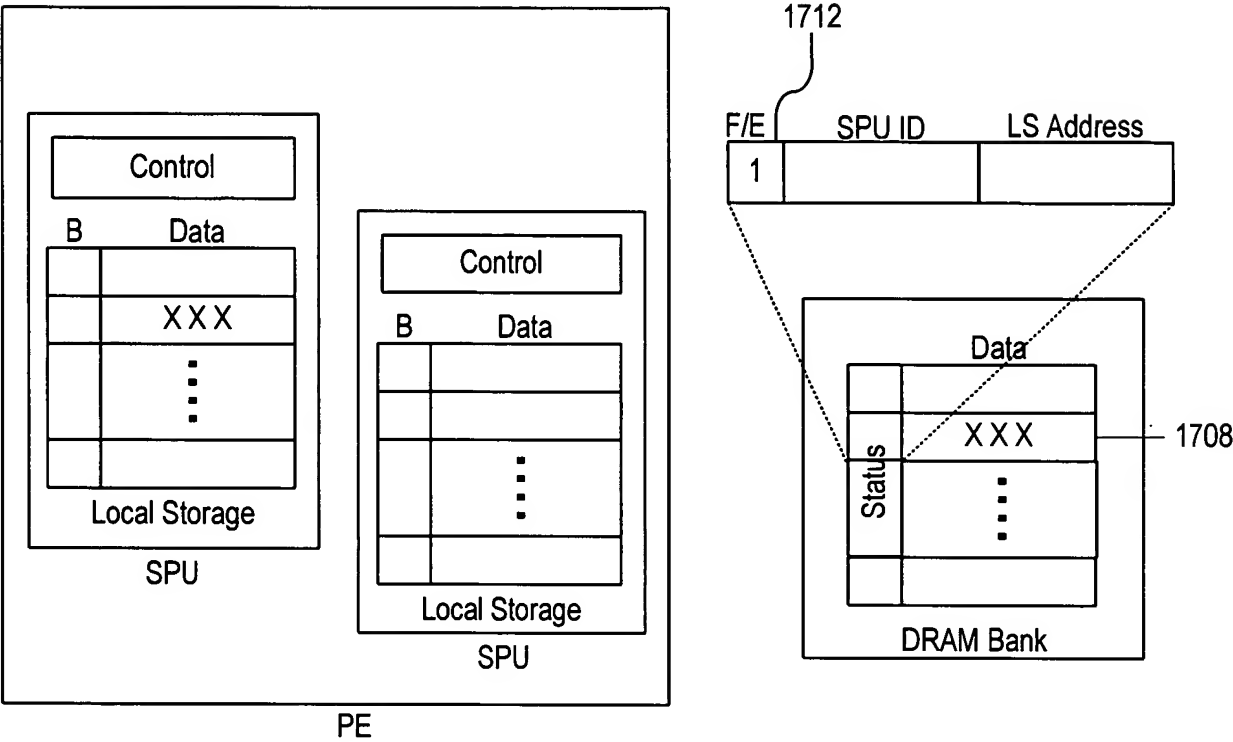


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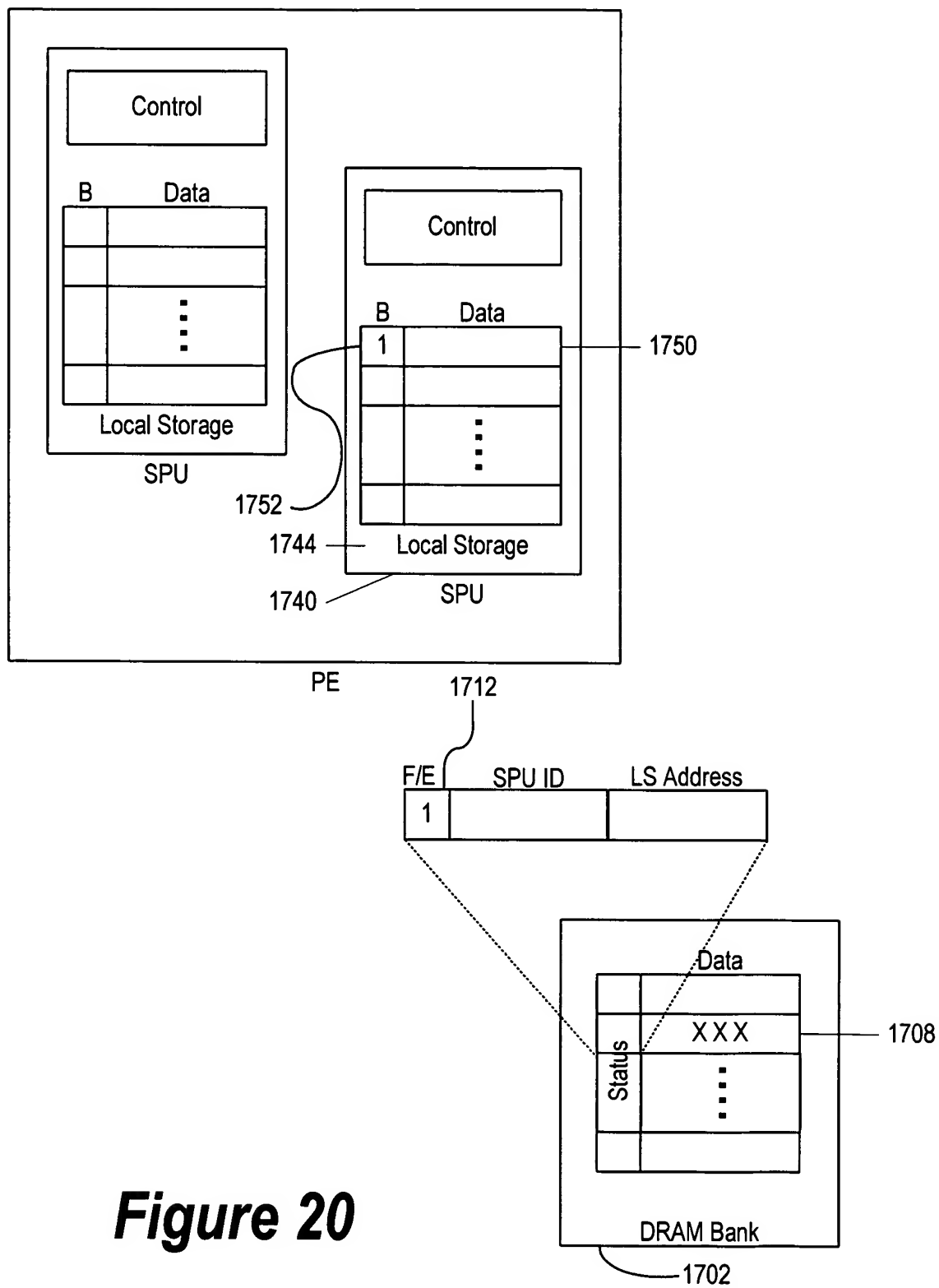


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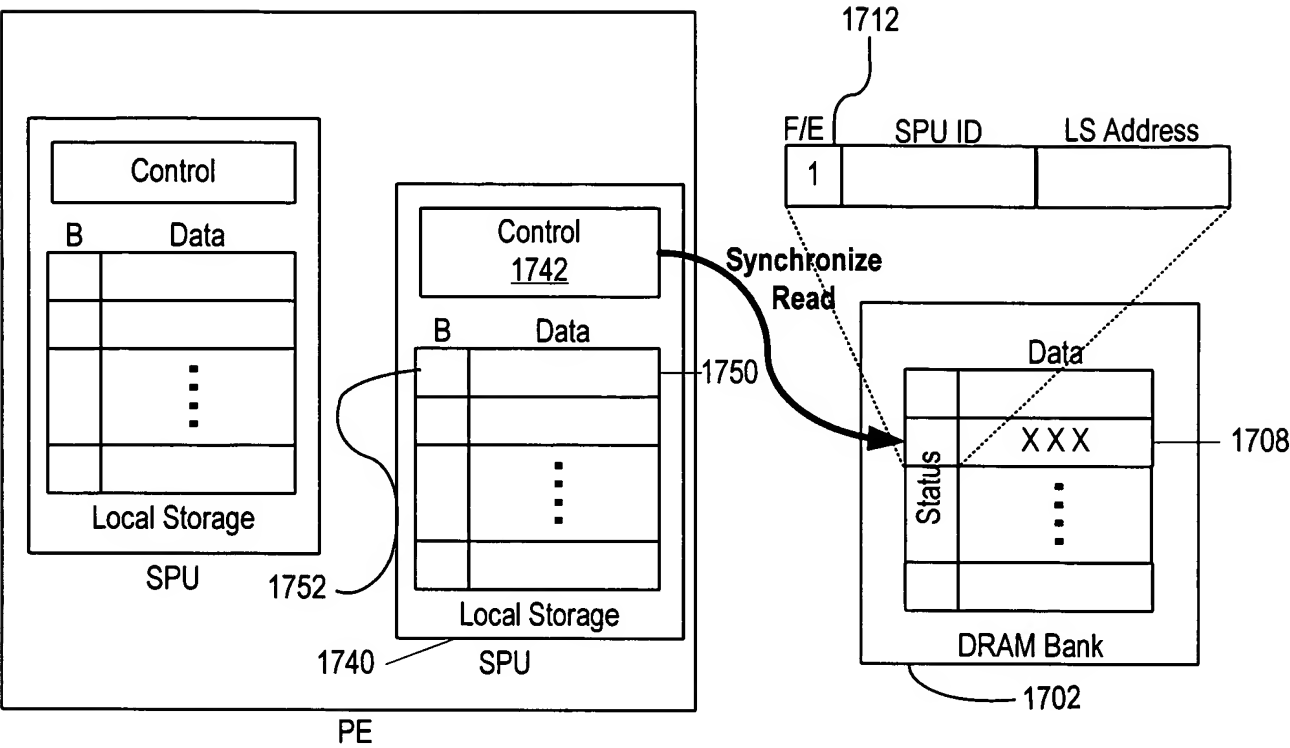


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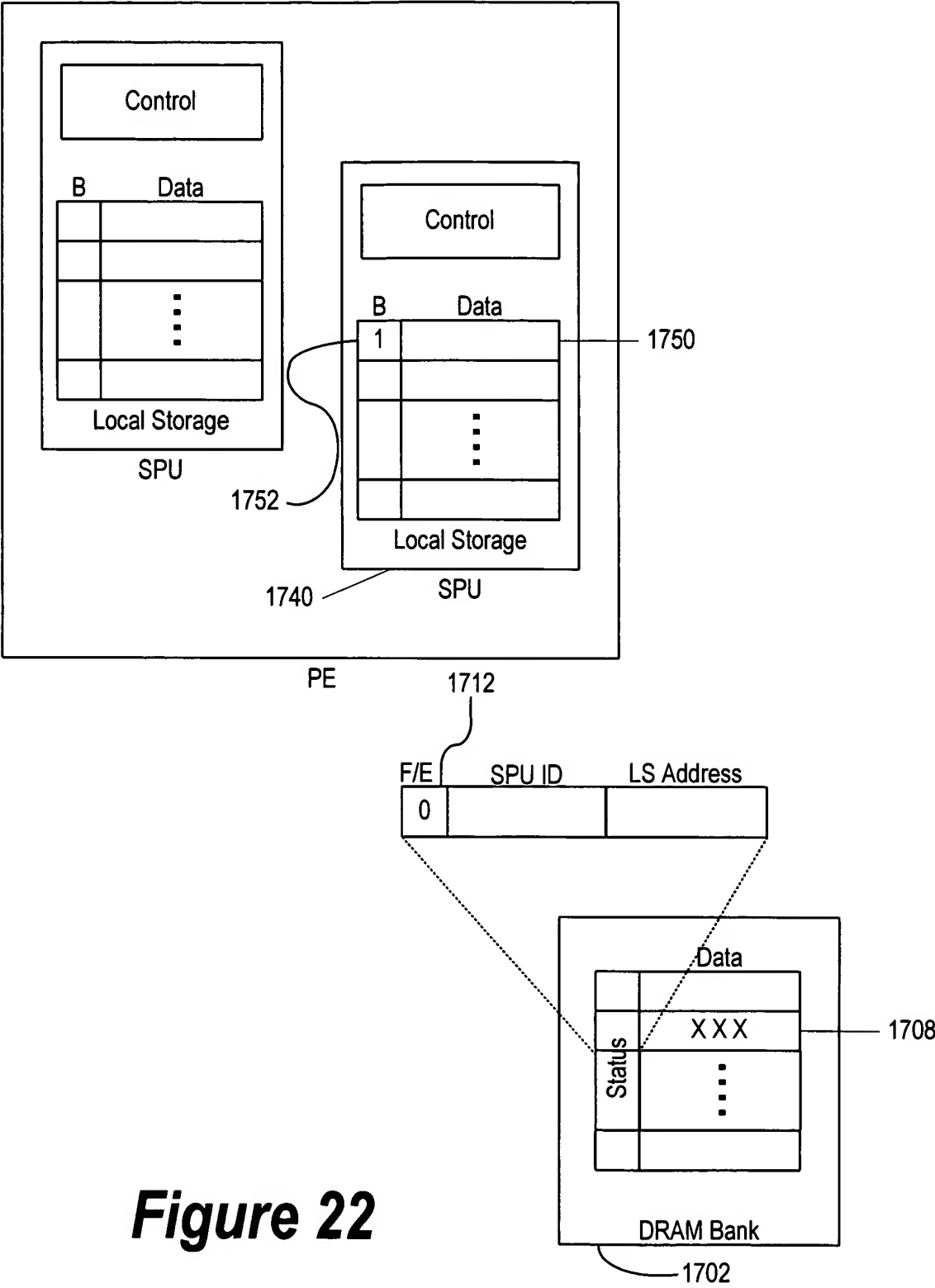


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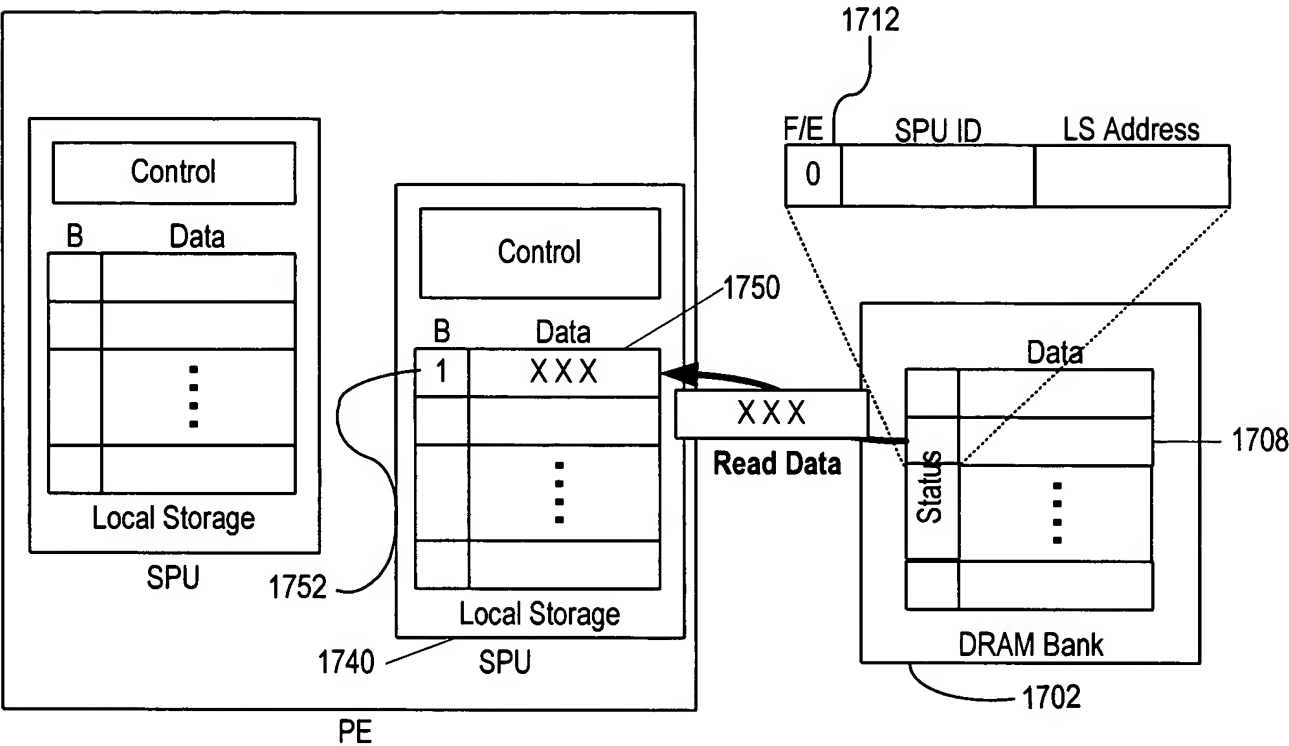


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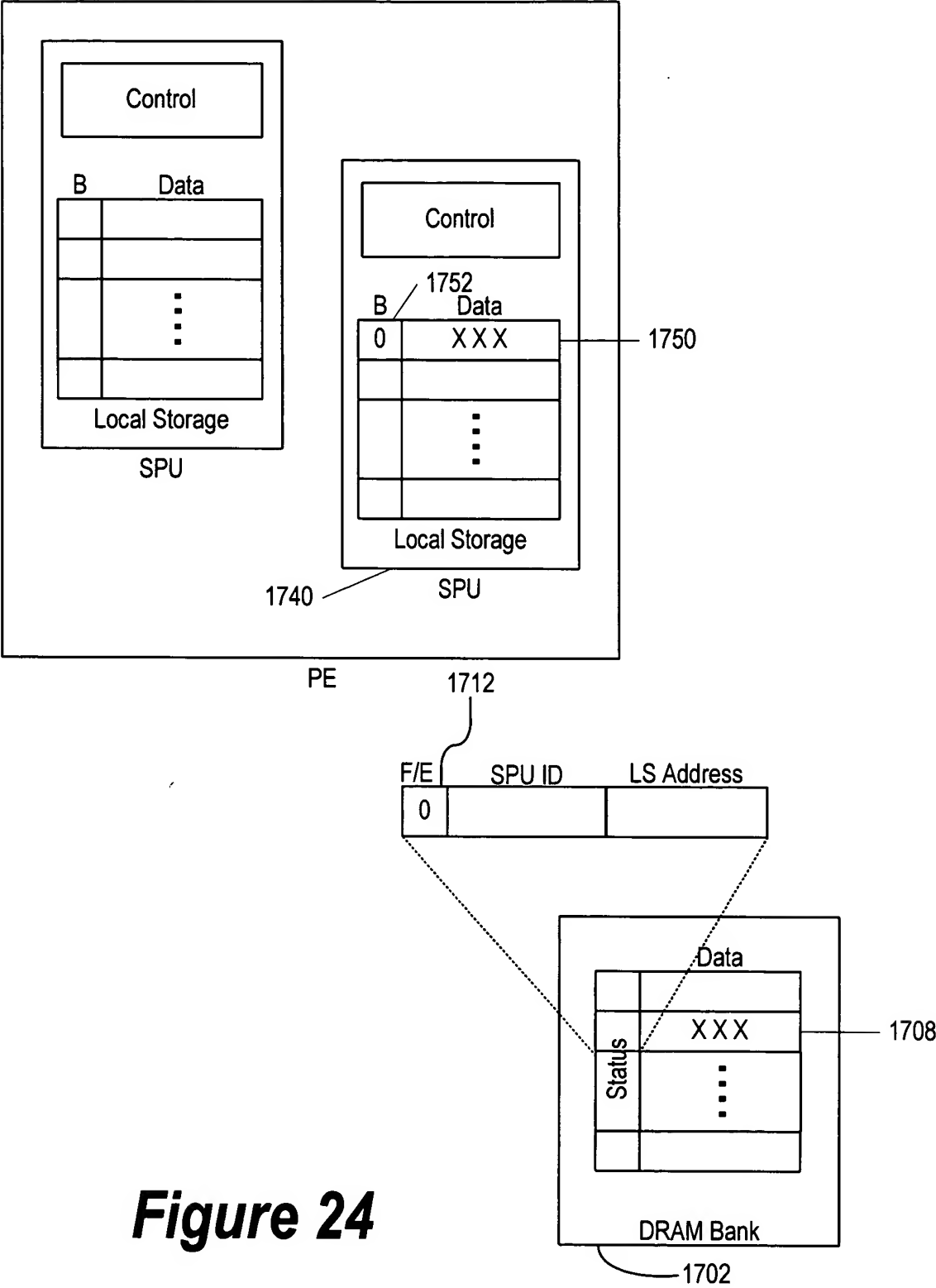


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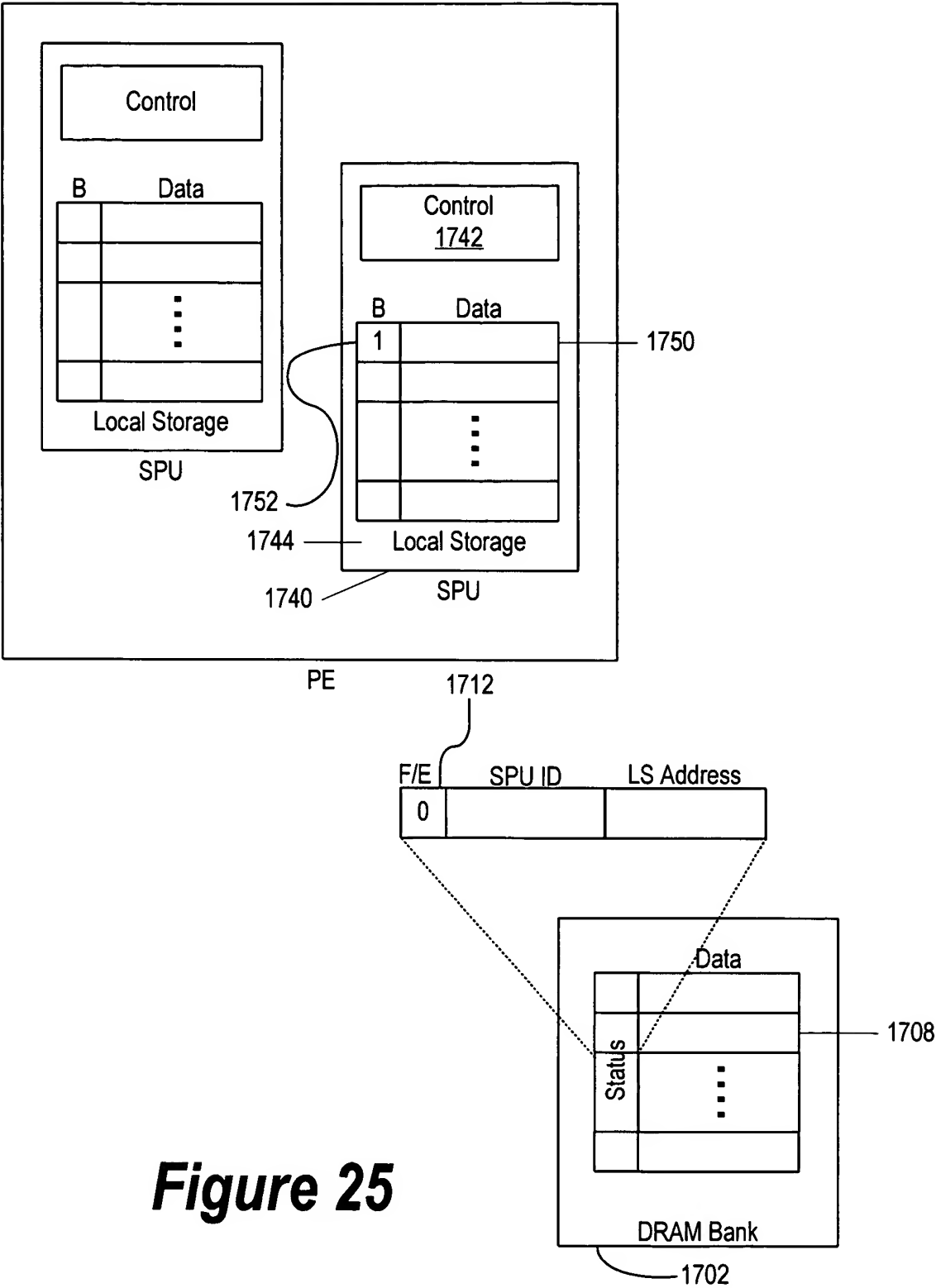


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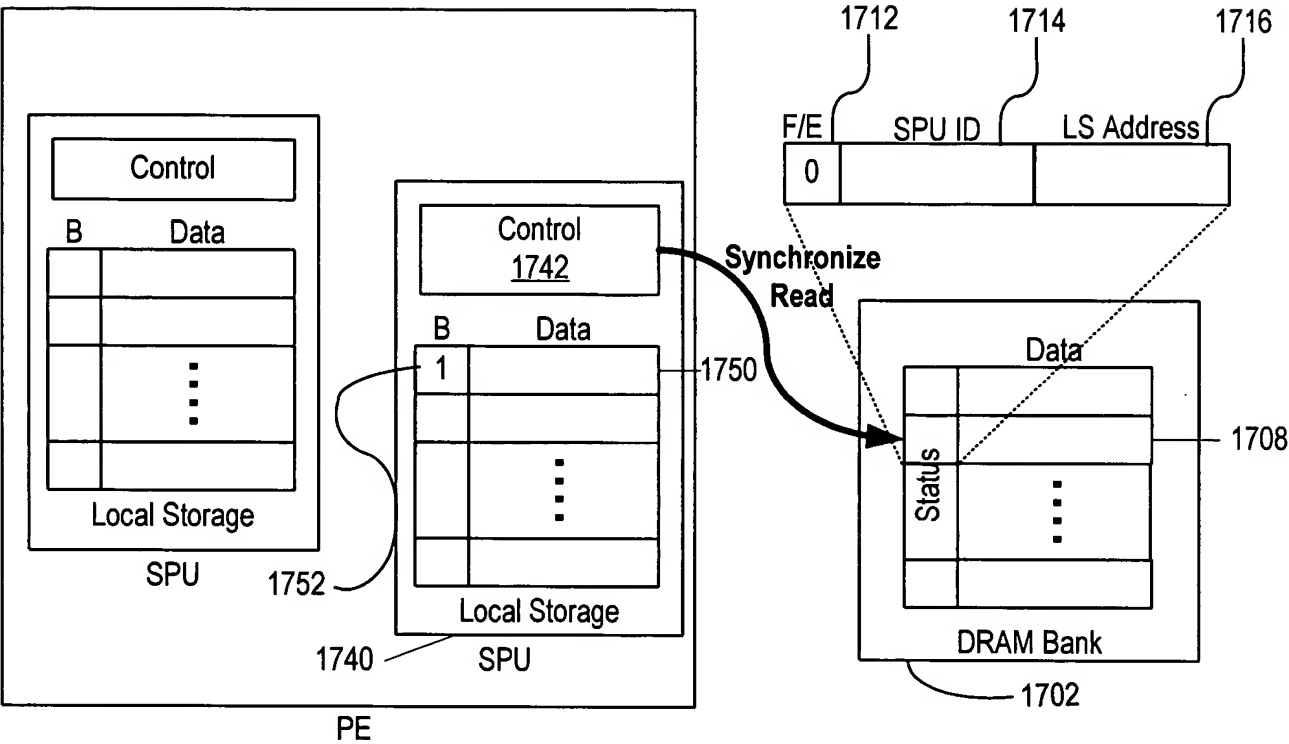


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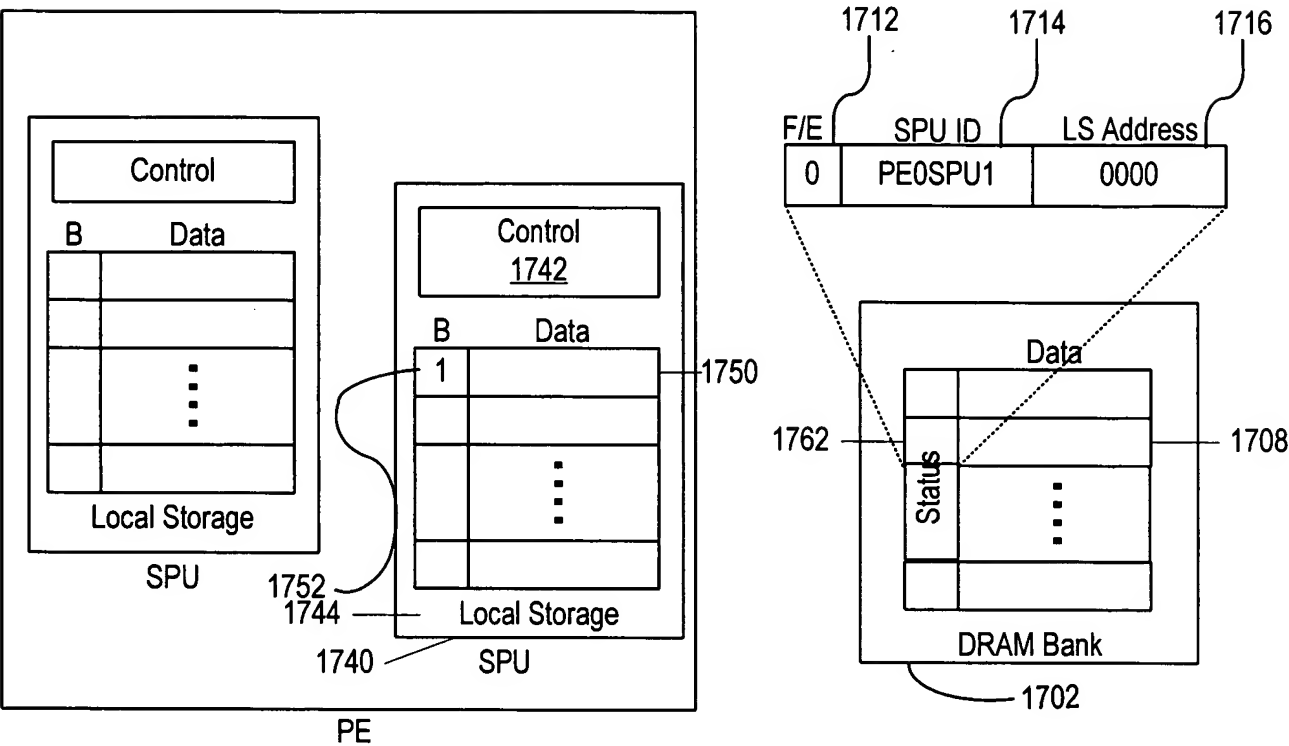


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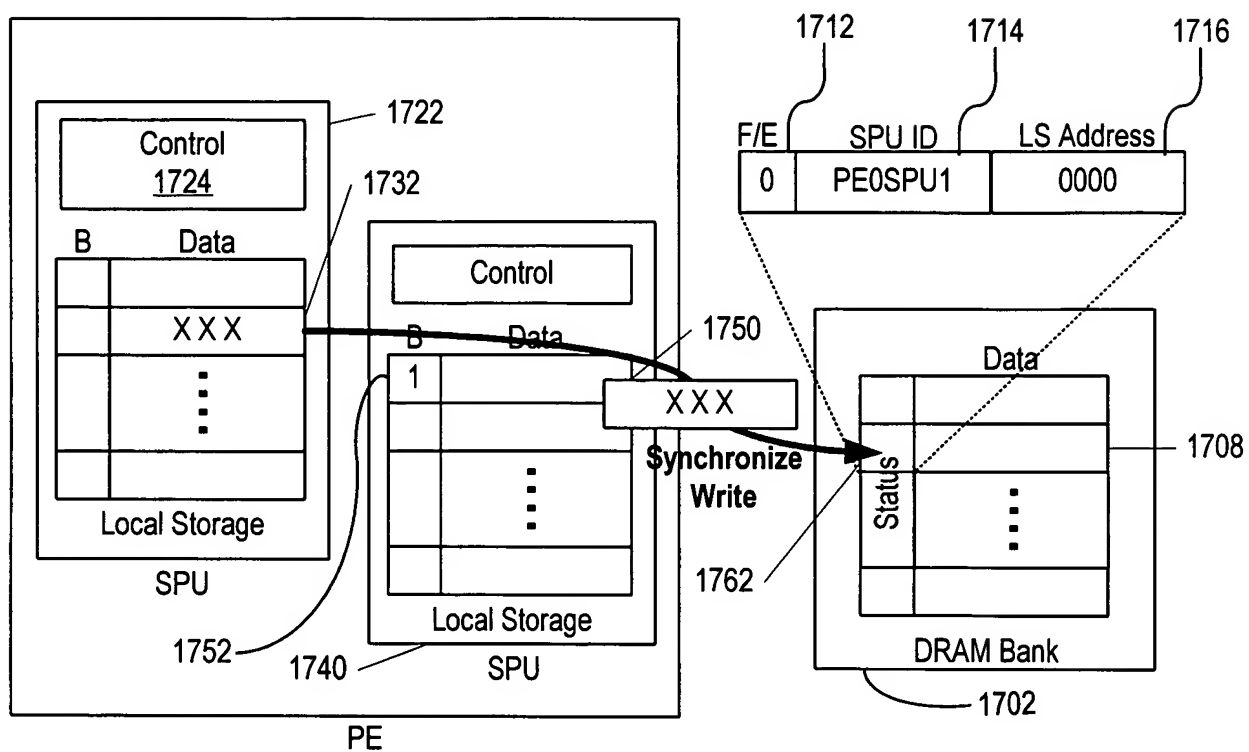


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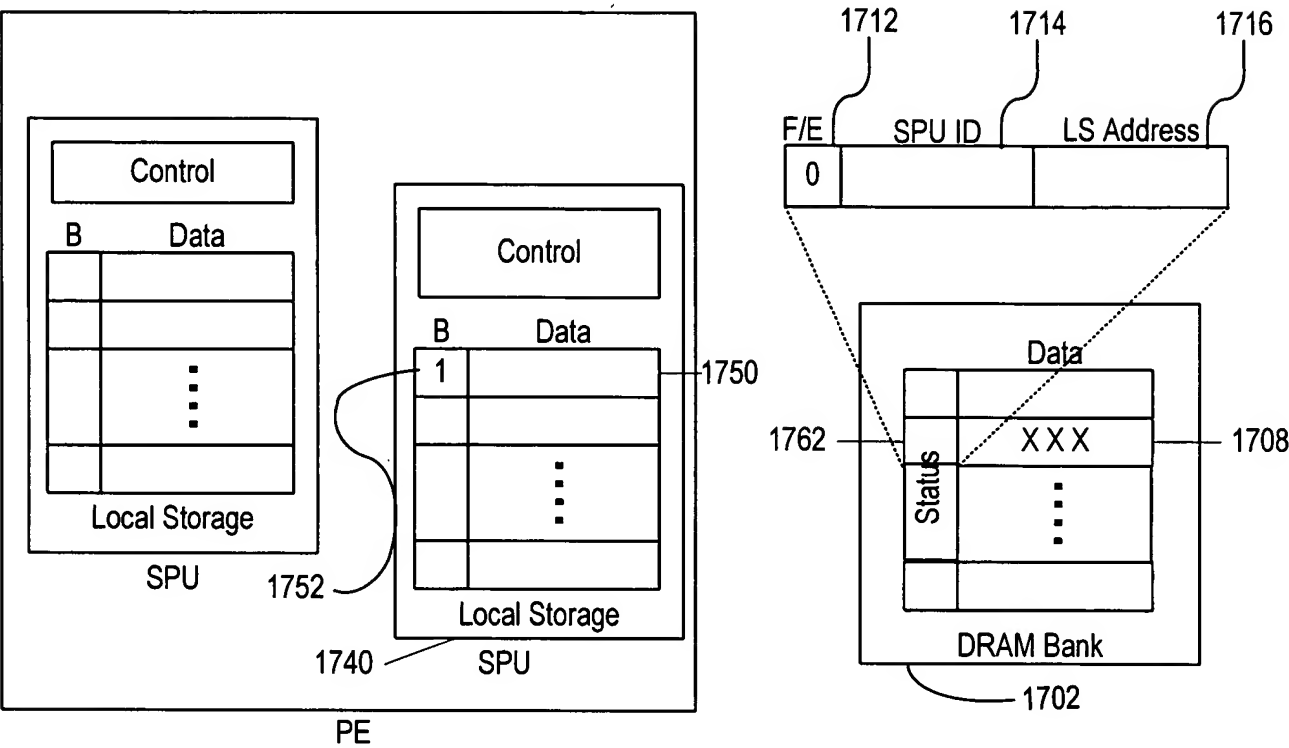


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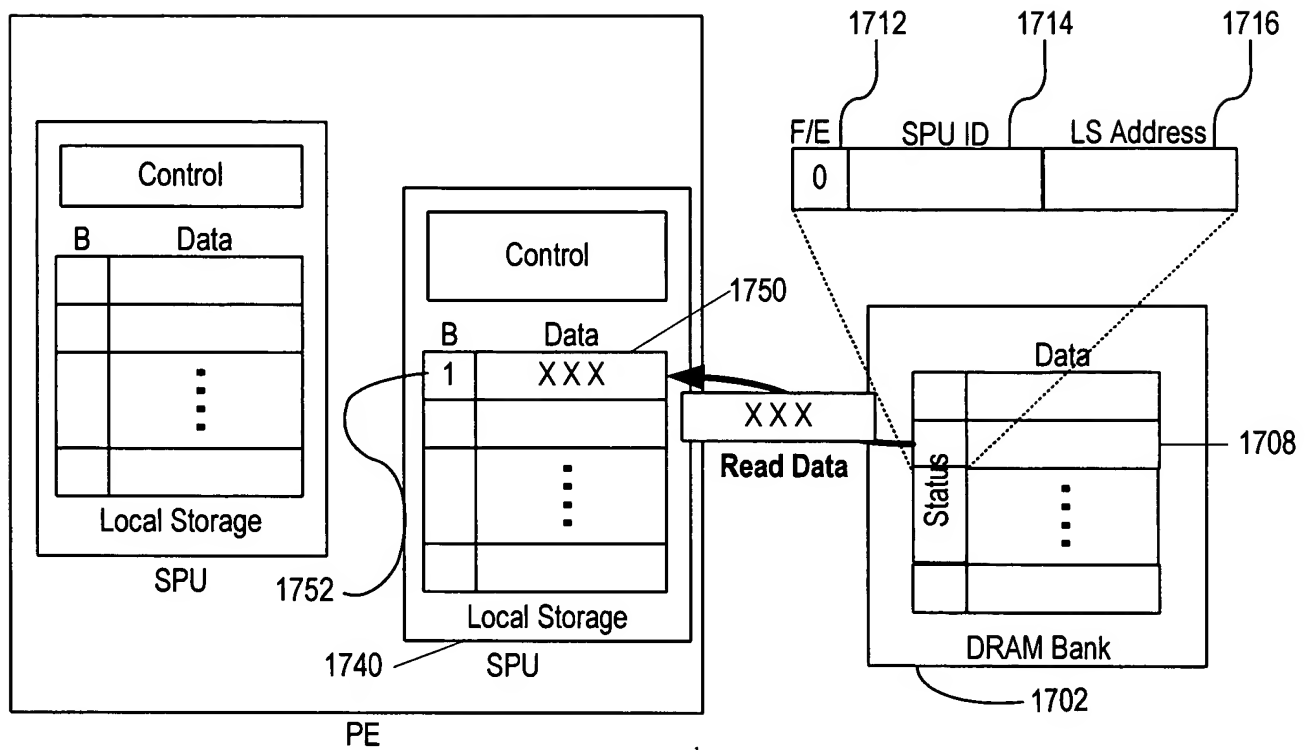


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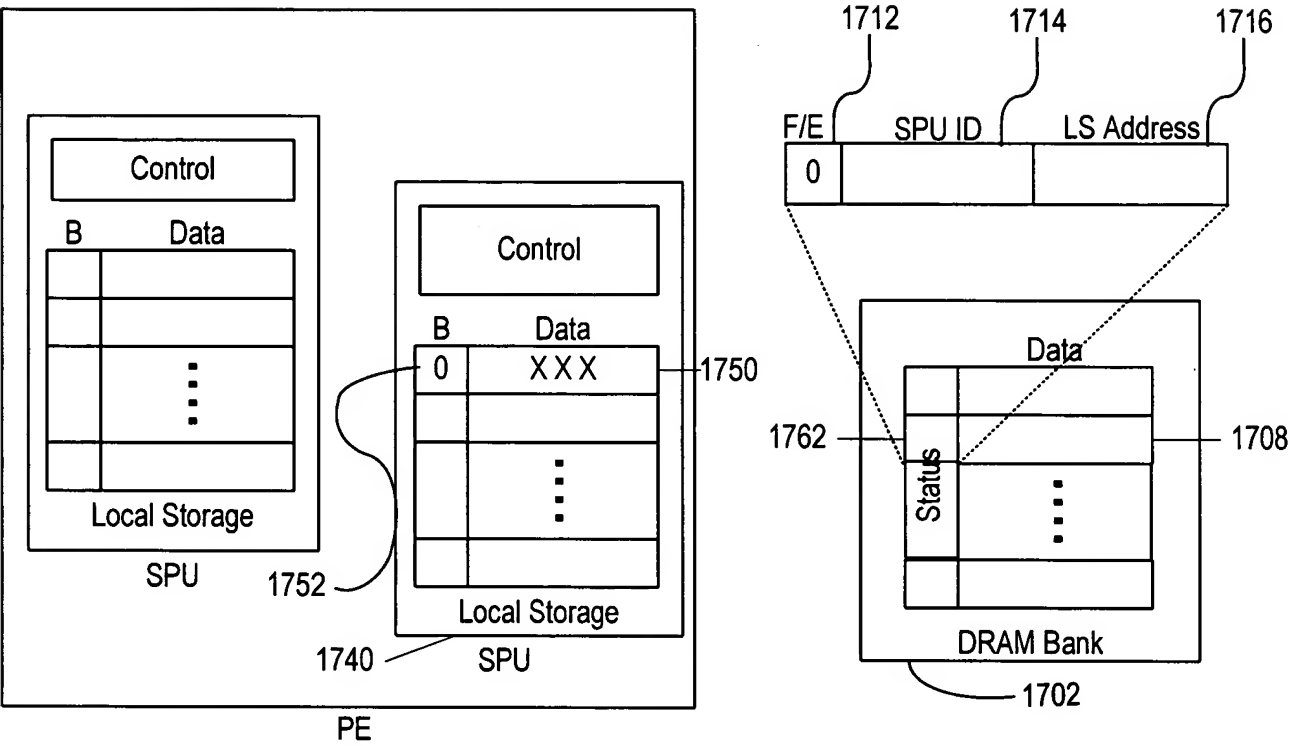


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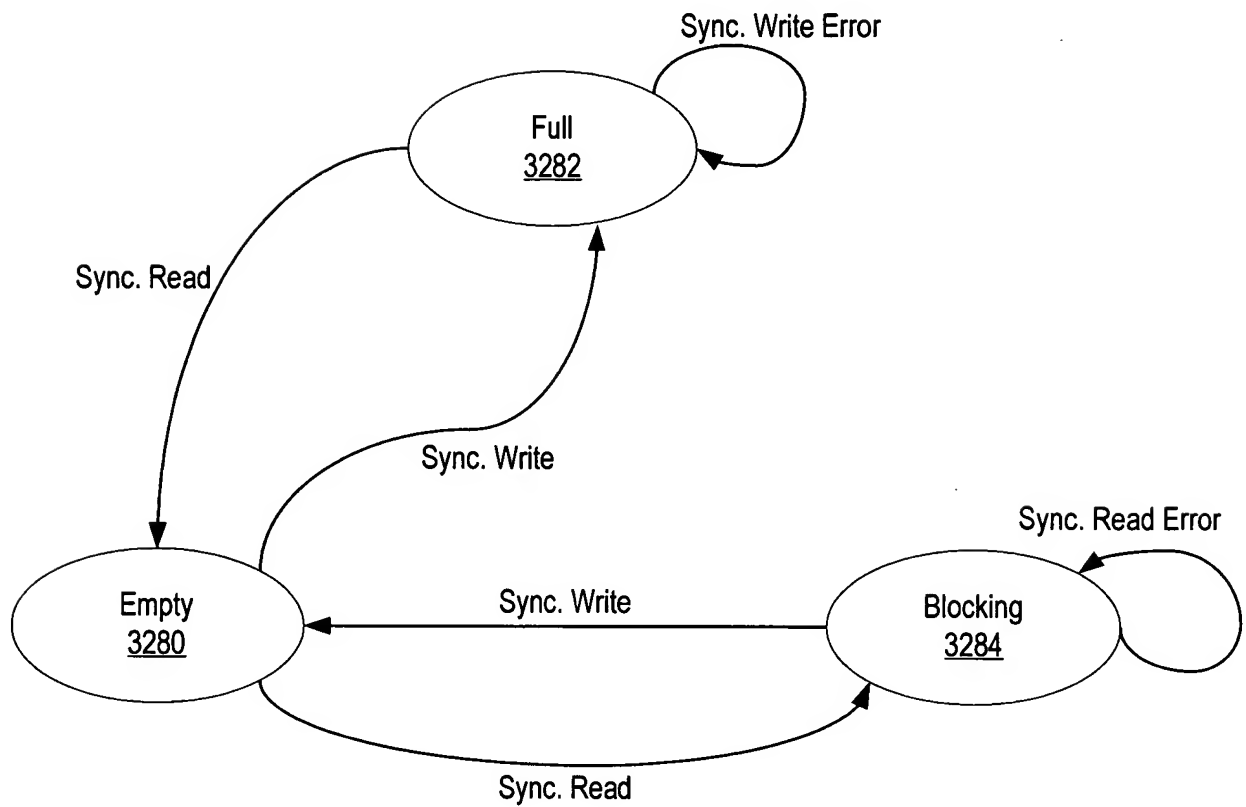


Figure 32

Key Control Table

3302

3304 ID 3306 3308

0	SPU Key	Key Mask
1	SPU Key	Key Mask
2	SPU Key	Key Mask
	⋮	
7	SPU Key	Key Mask

Figure 33

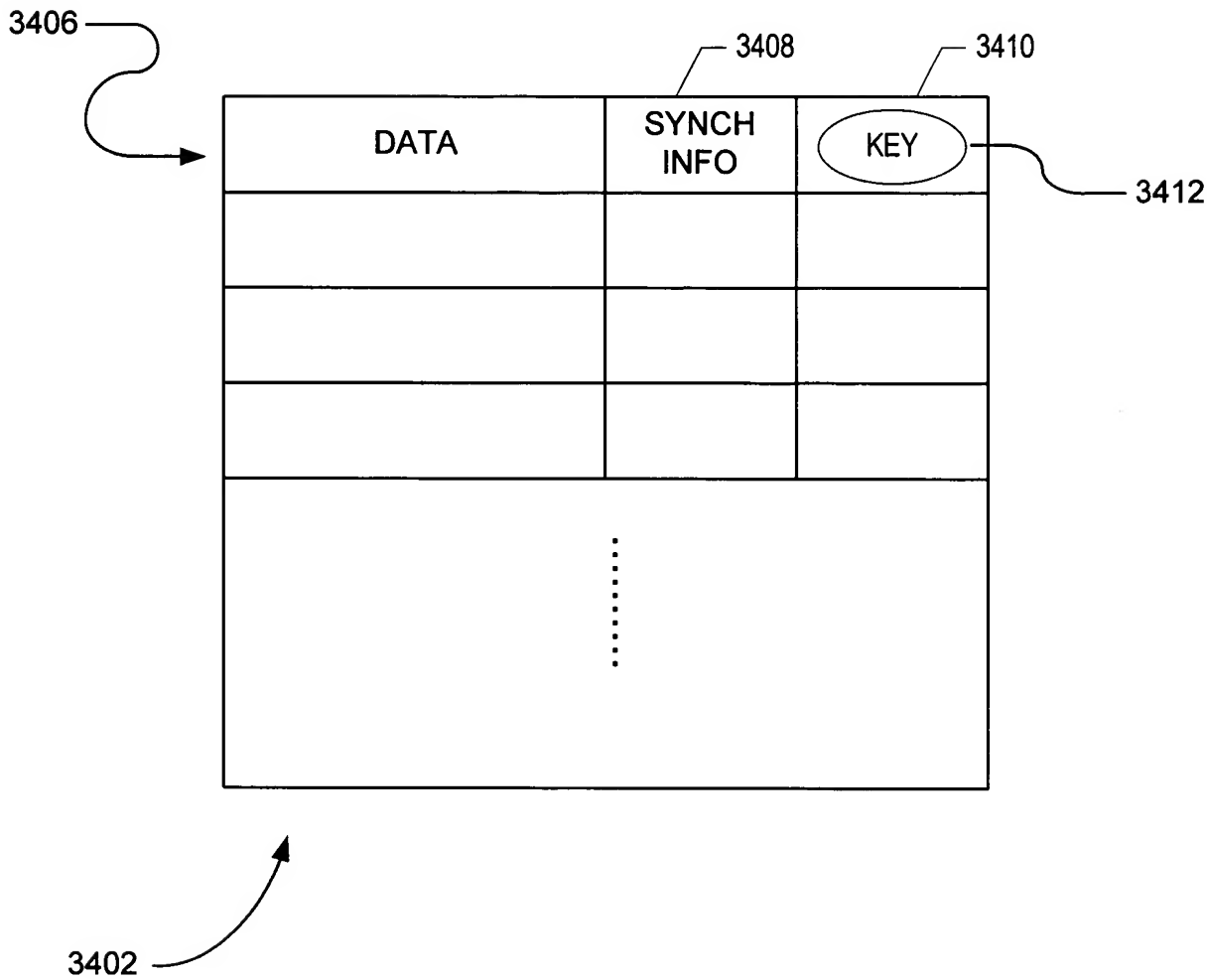


Figure 34

Memory Access Control Table

3504

3506

3508

3510

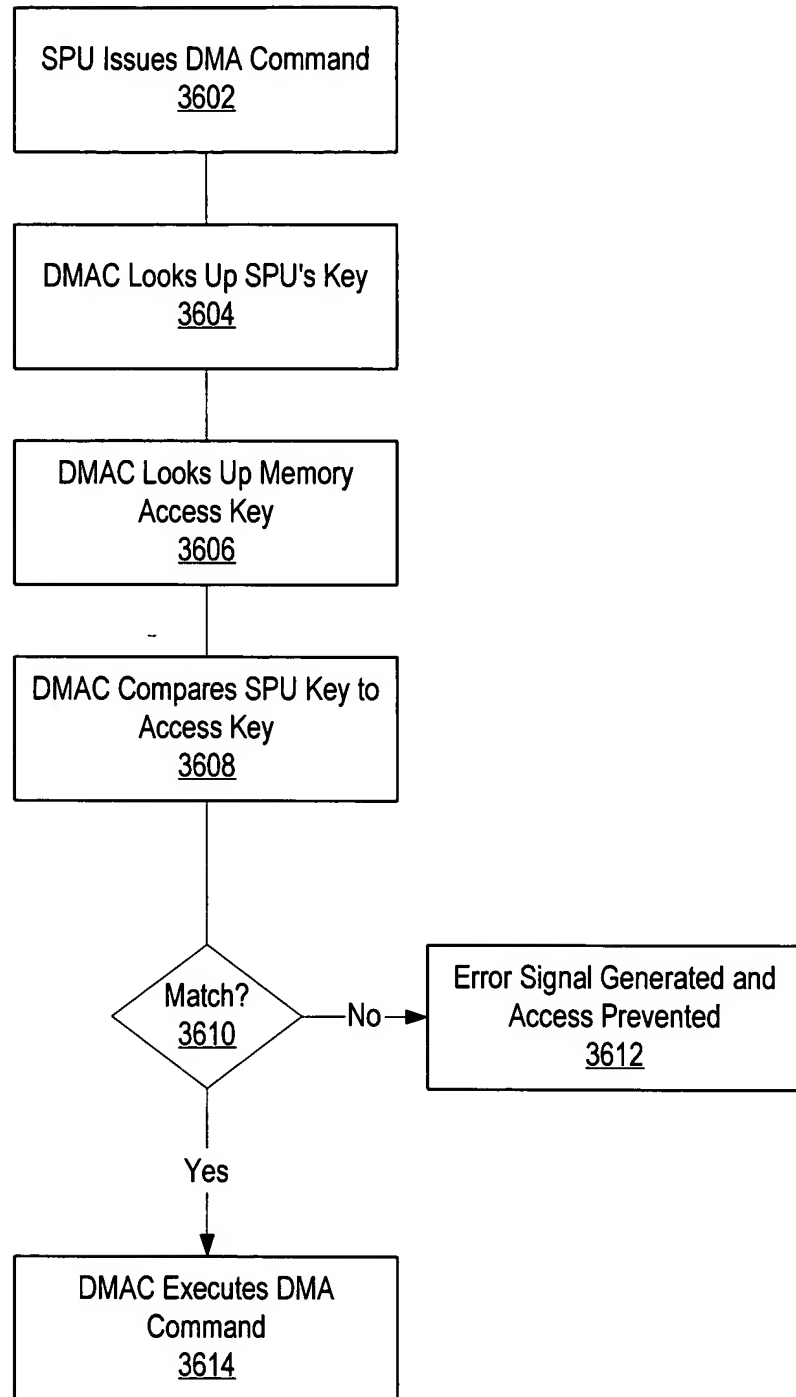
3512

ID	Base	Size	Access Key	Access Key Mask
0	Base	Size	Access Key	Access Key Mask
1	Base	Size	Access Key	Access Key Mask
2	Base	Size	Access Key	Access Key Mask
	⋮			
63	Base	Size	Access Key	Access Key Mask

3502

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**Figure 36**

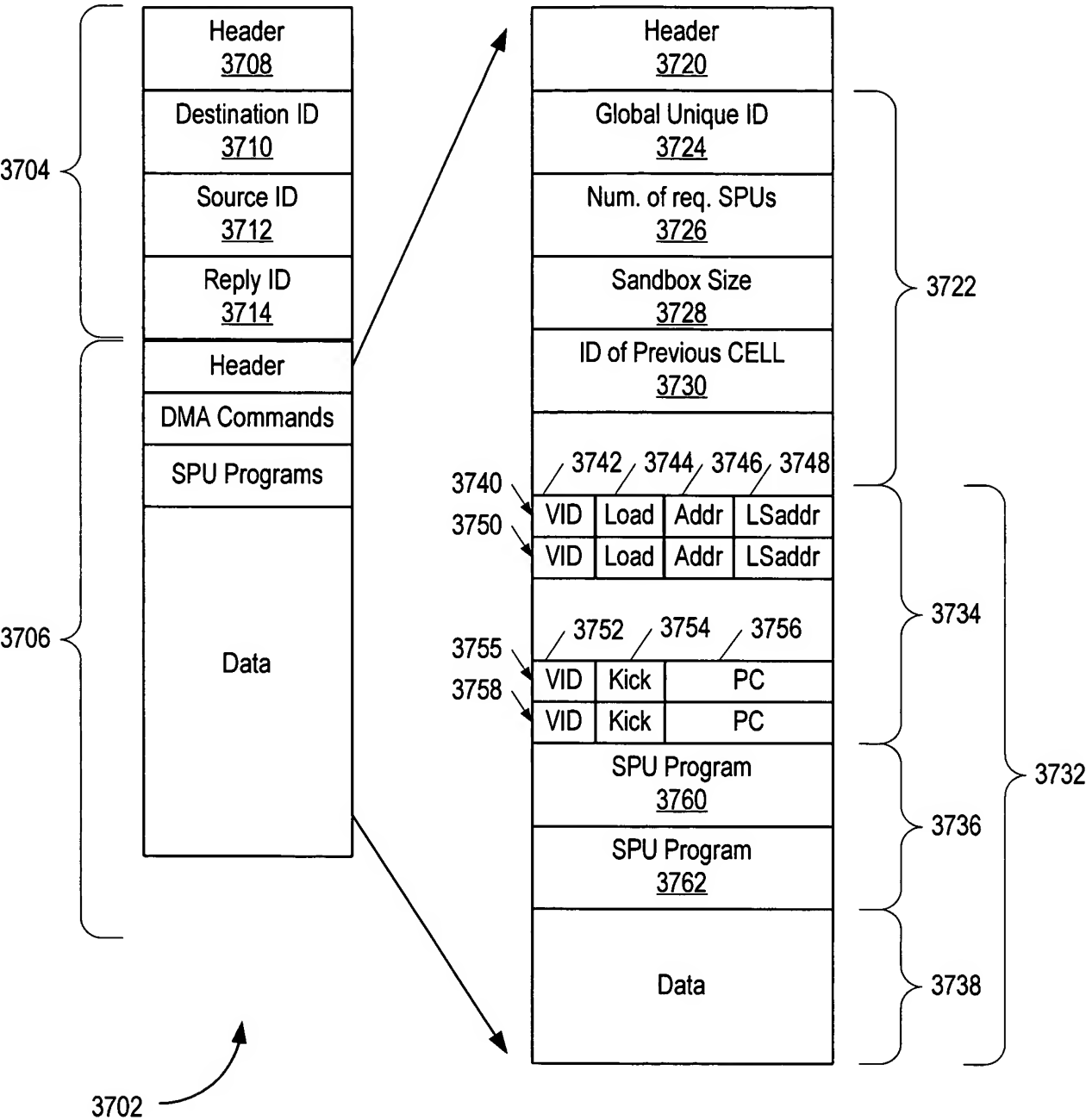


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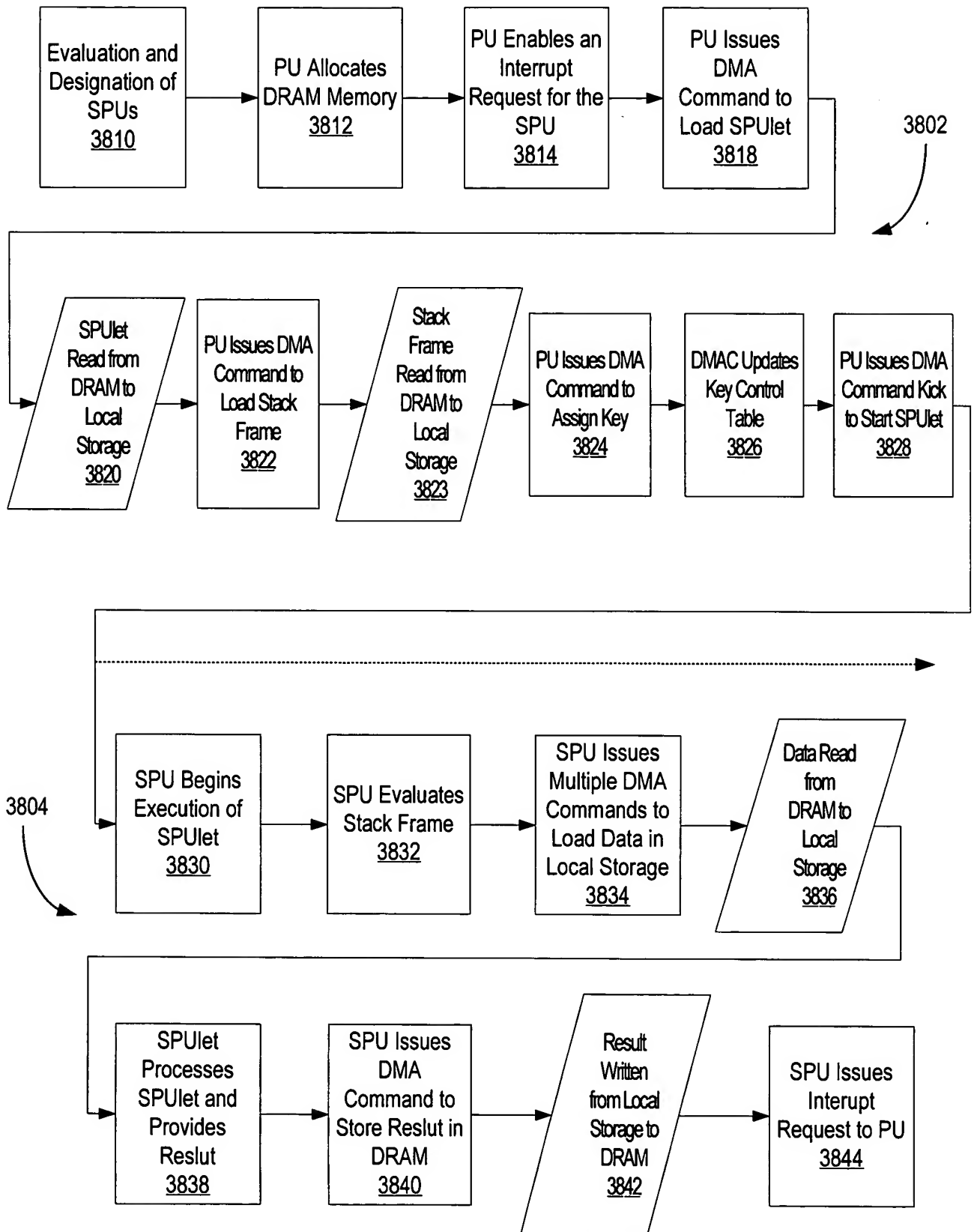
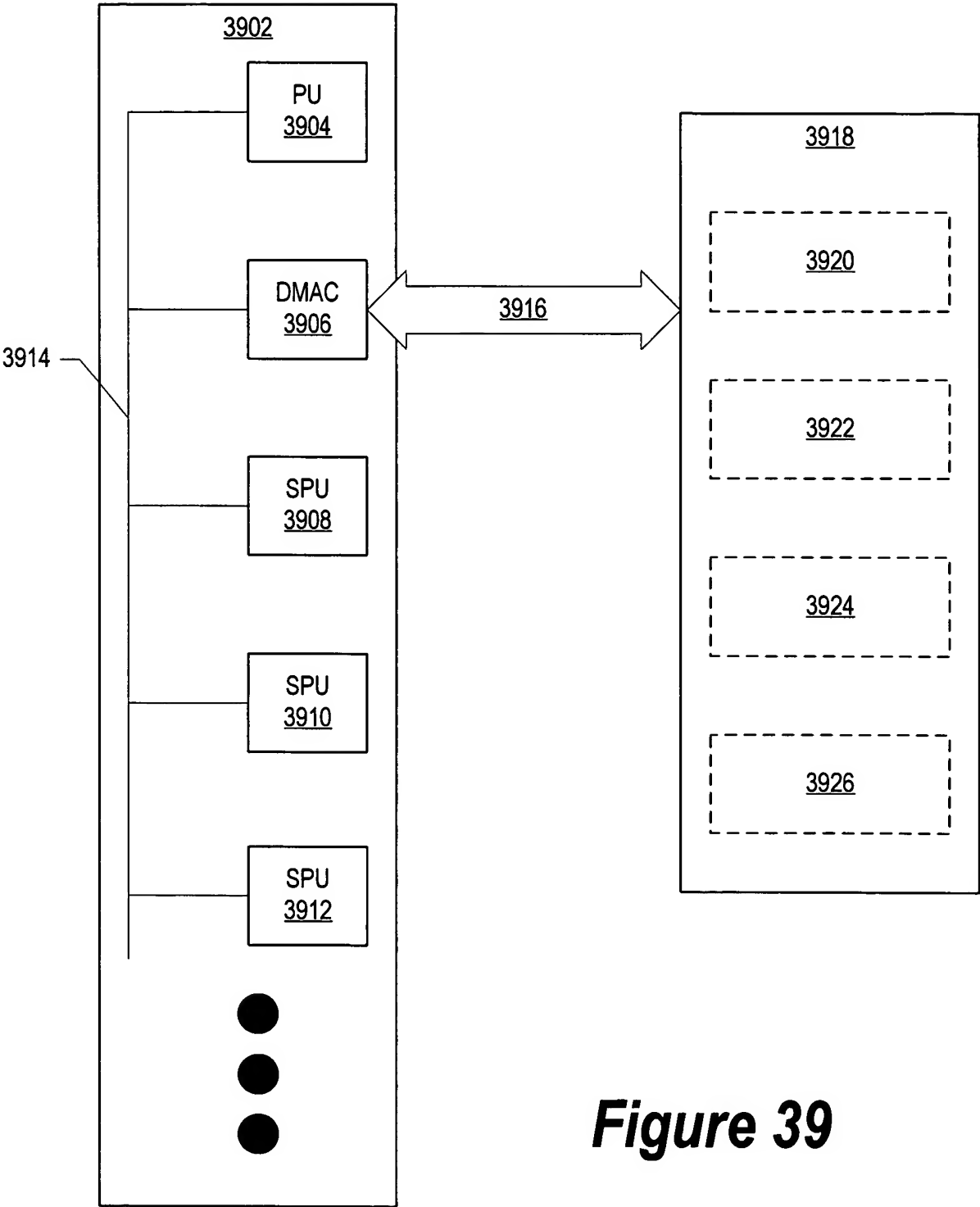
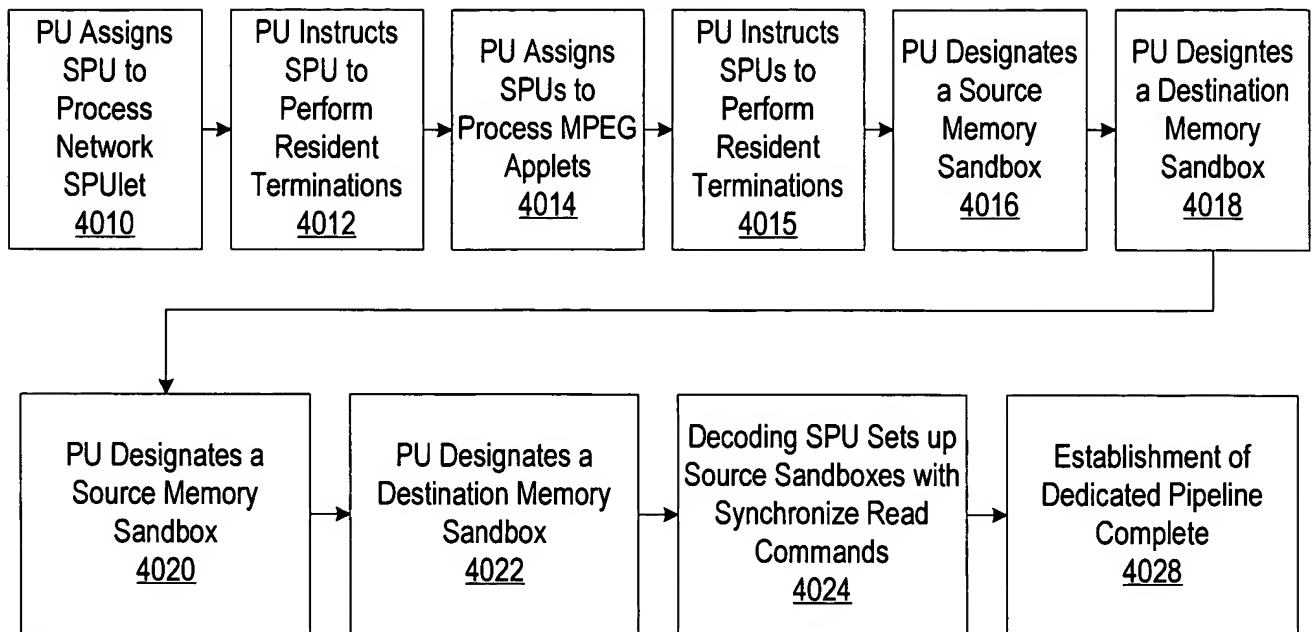
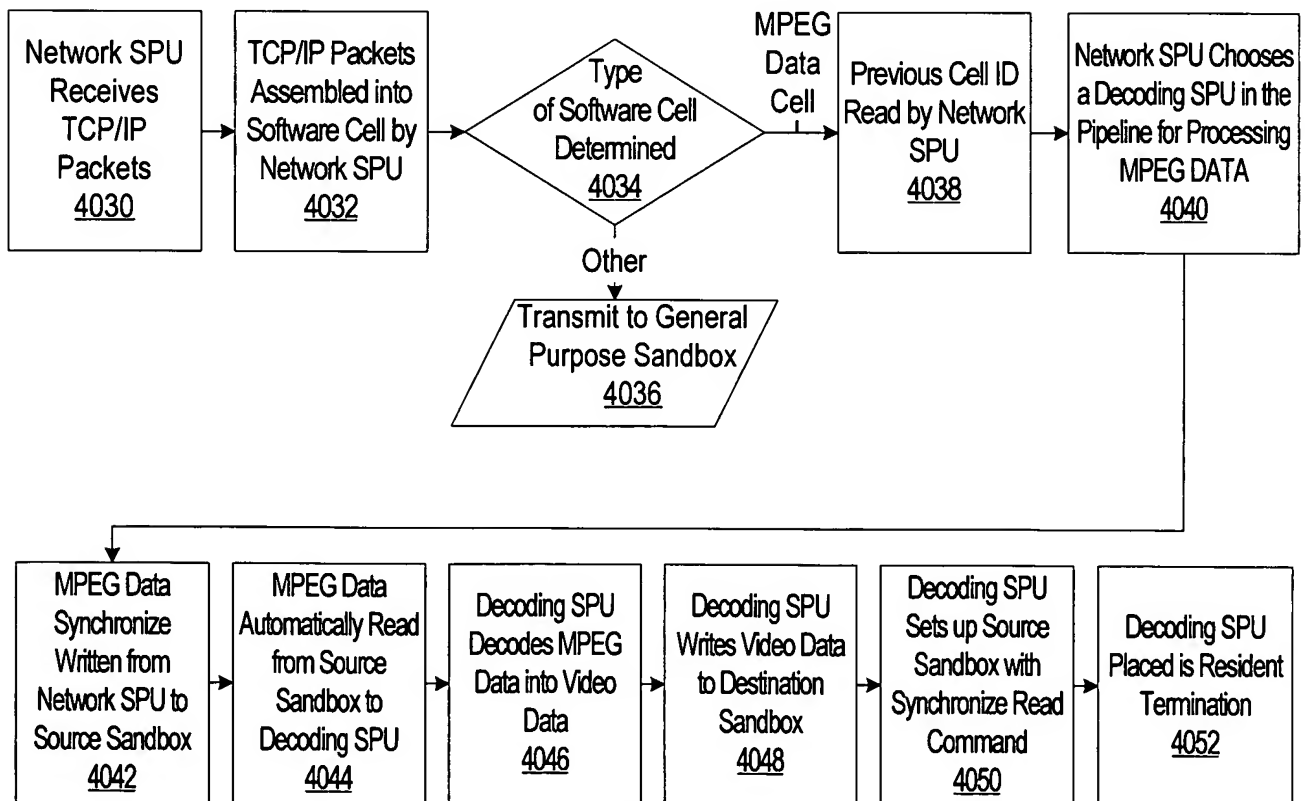


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**Figure 40A****Figure 40B**

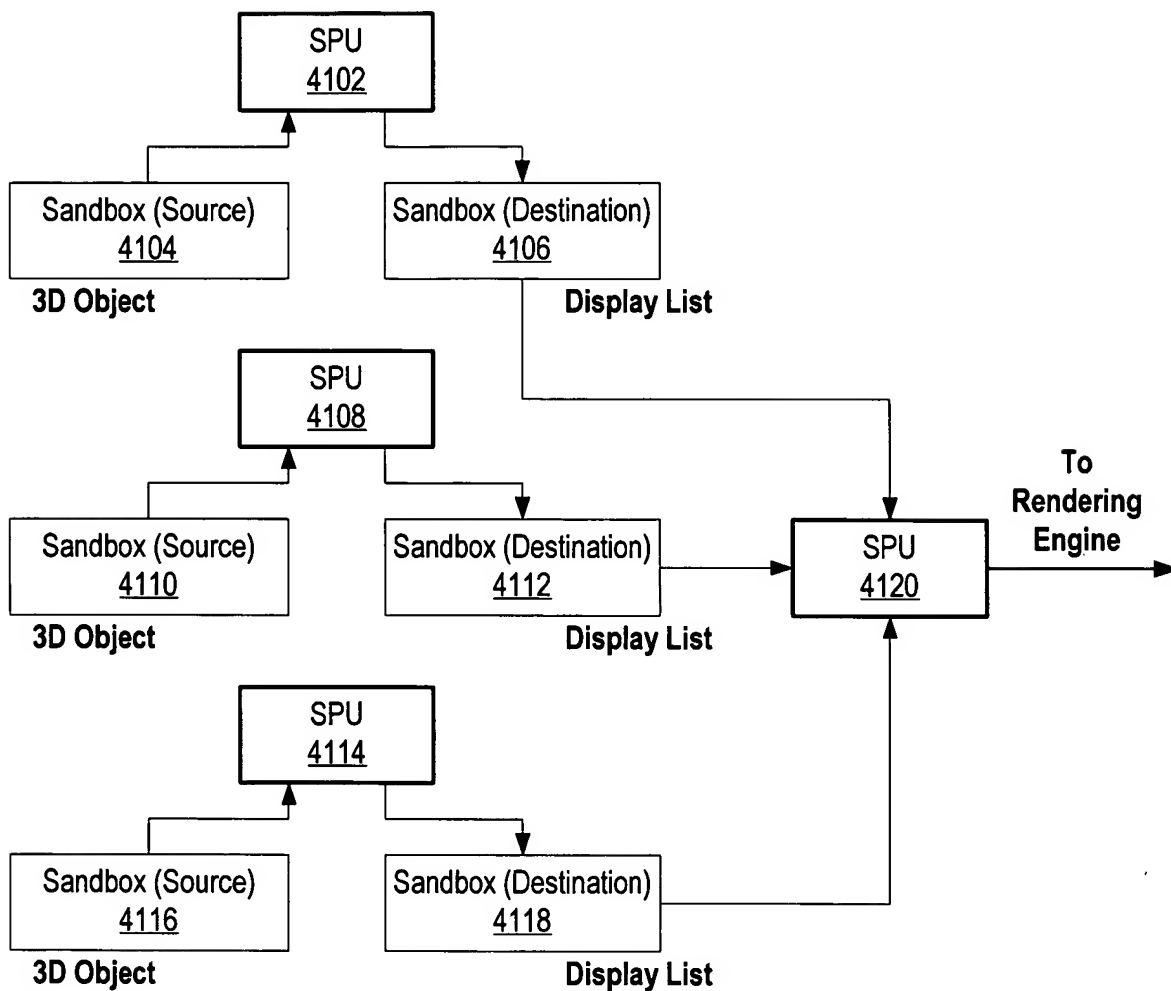


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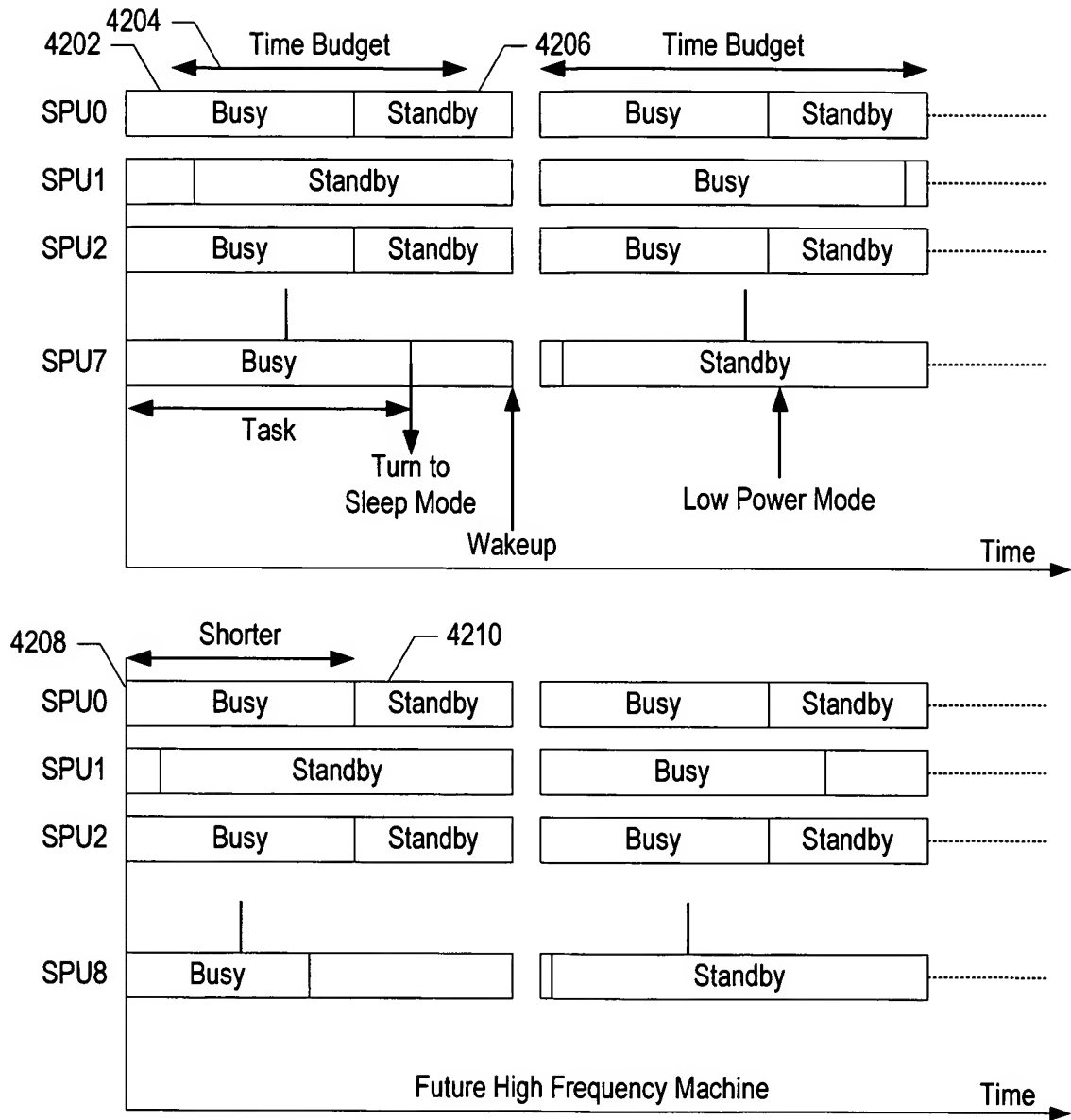
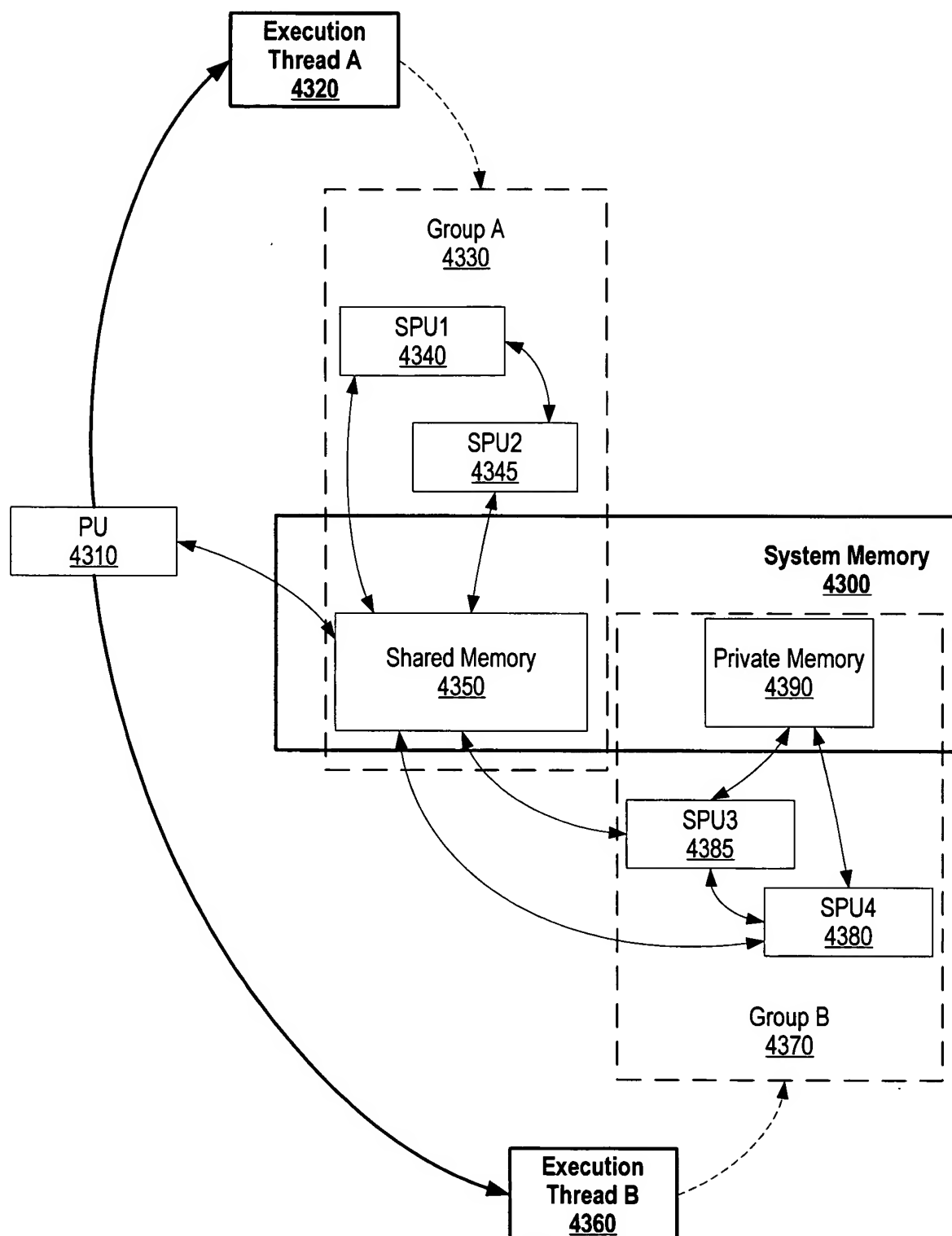
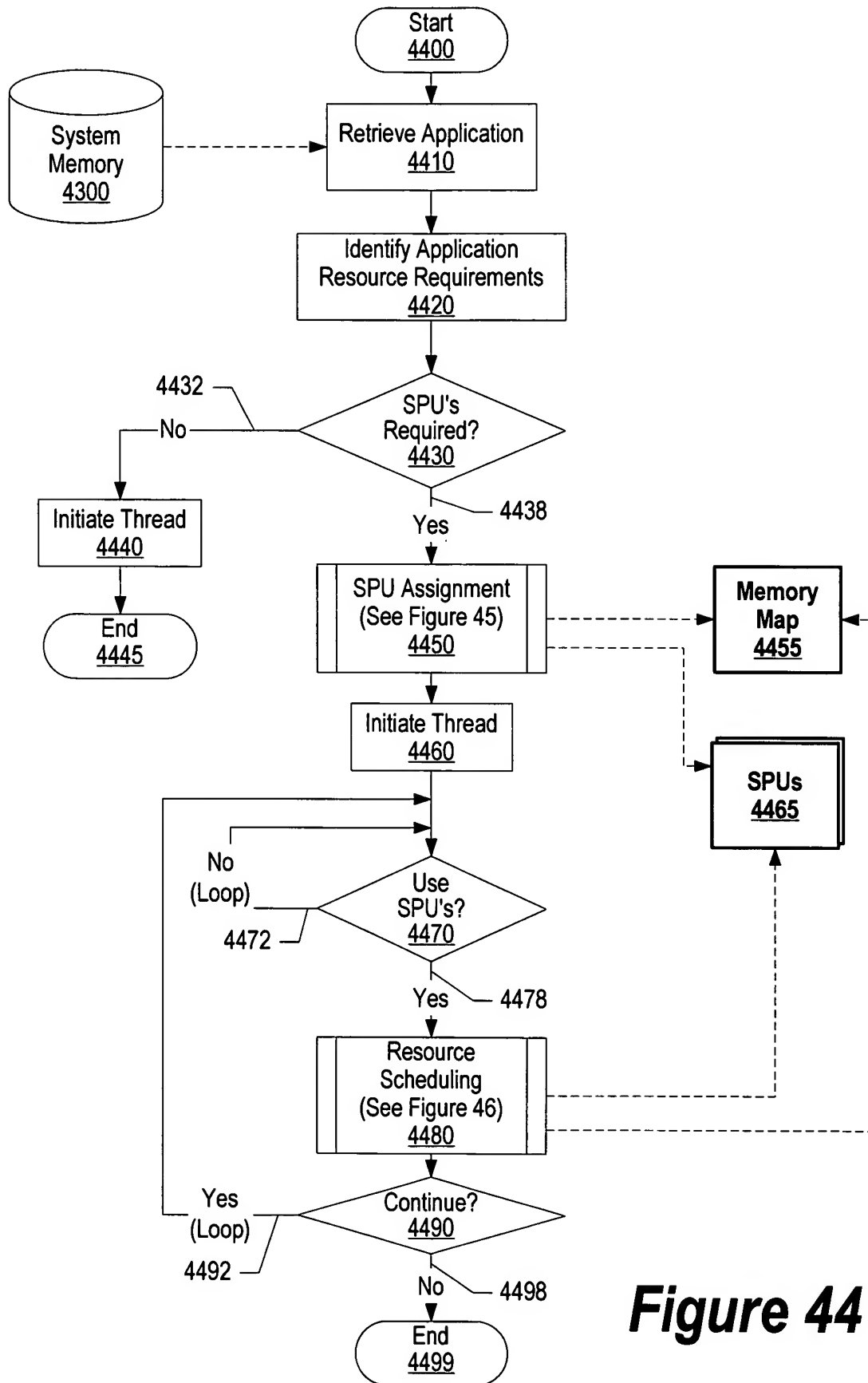


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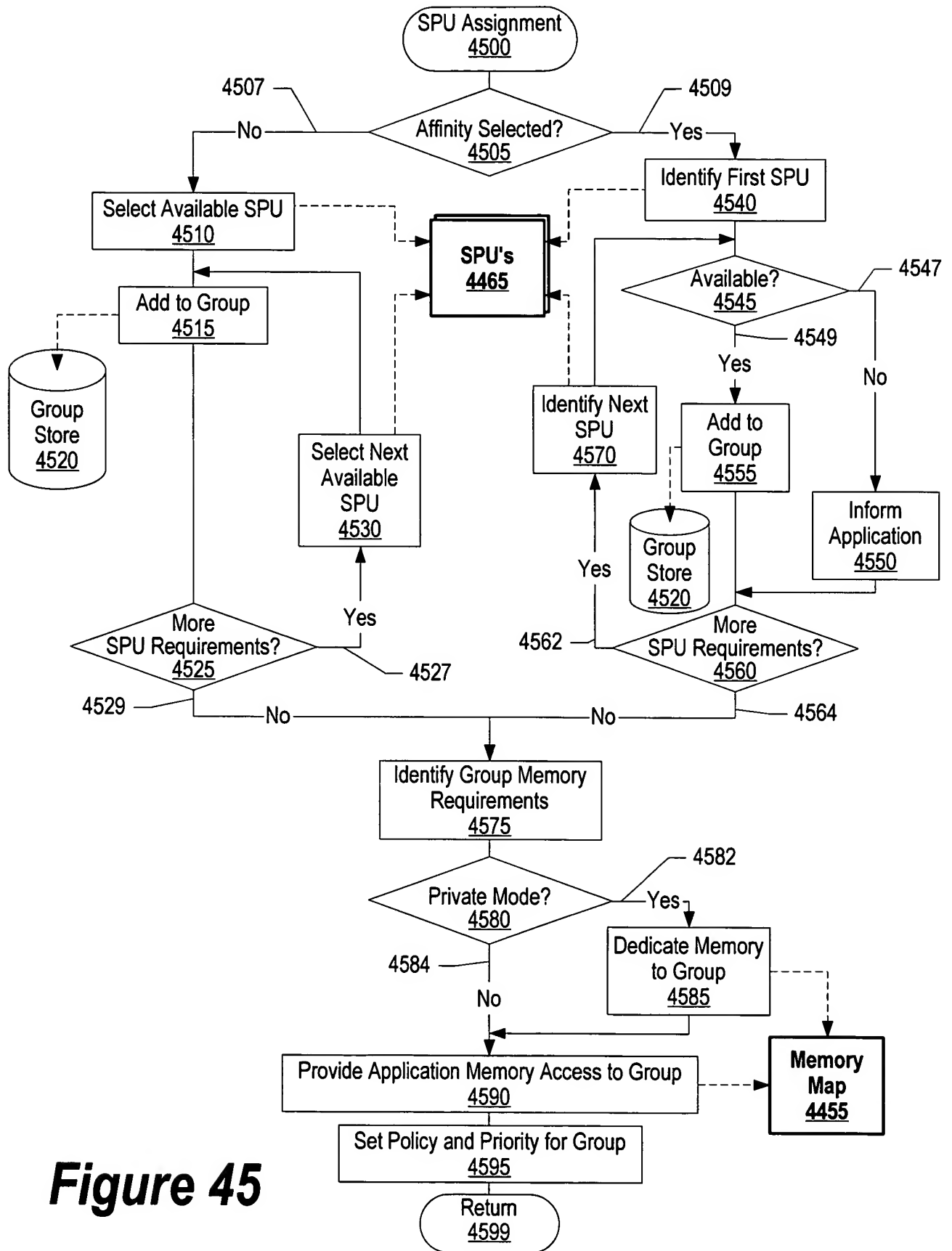
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**Figure 43**

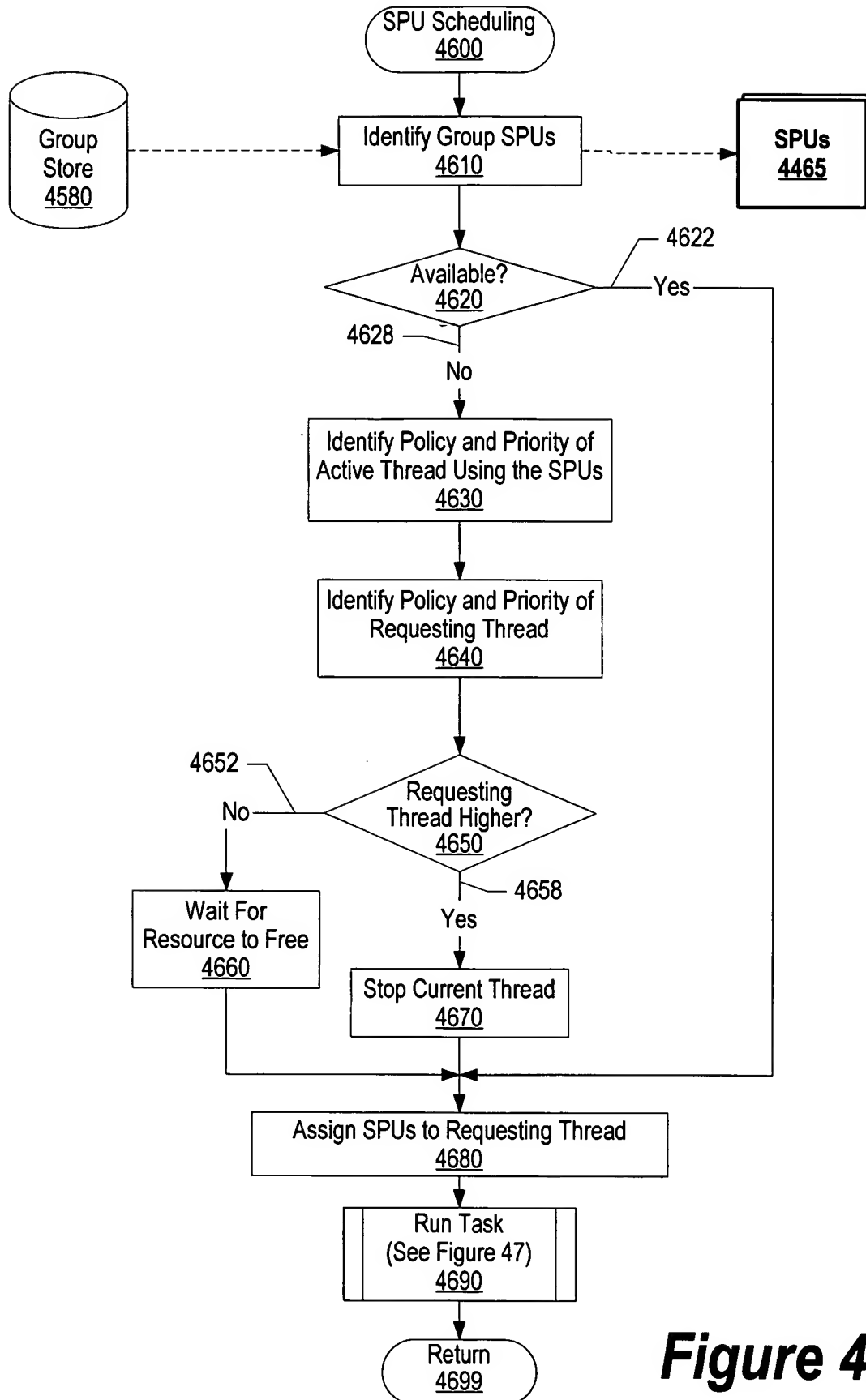
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**Figure 44**

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**Figure 45**

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**Figure 46**

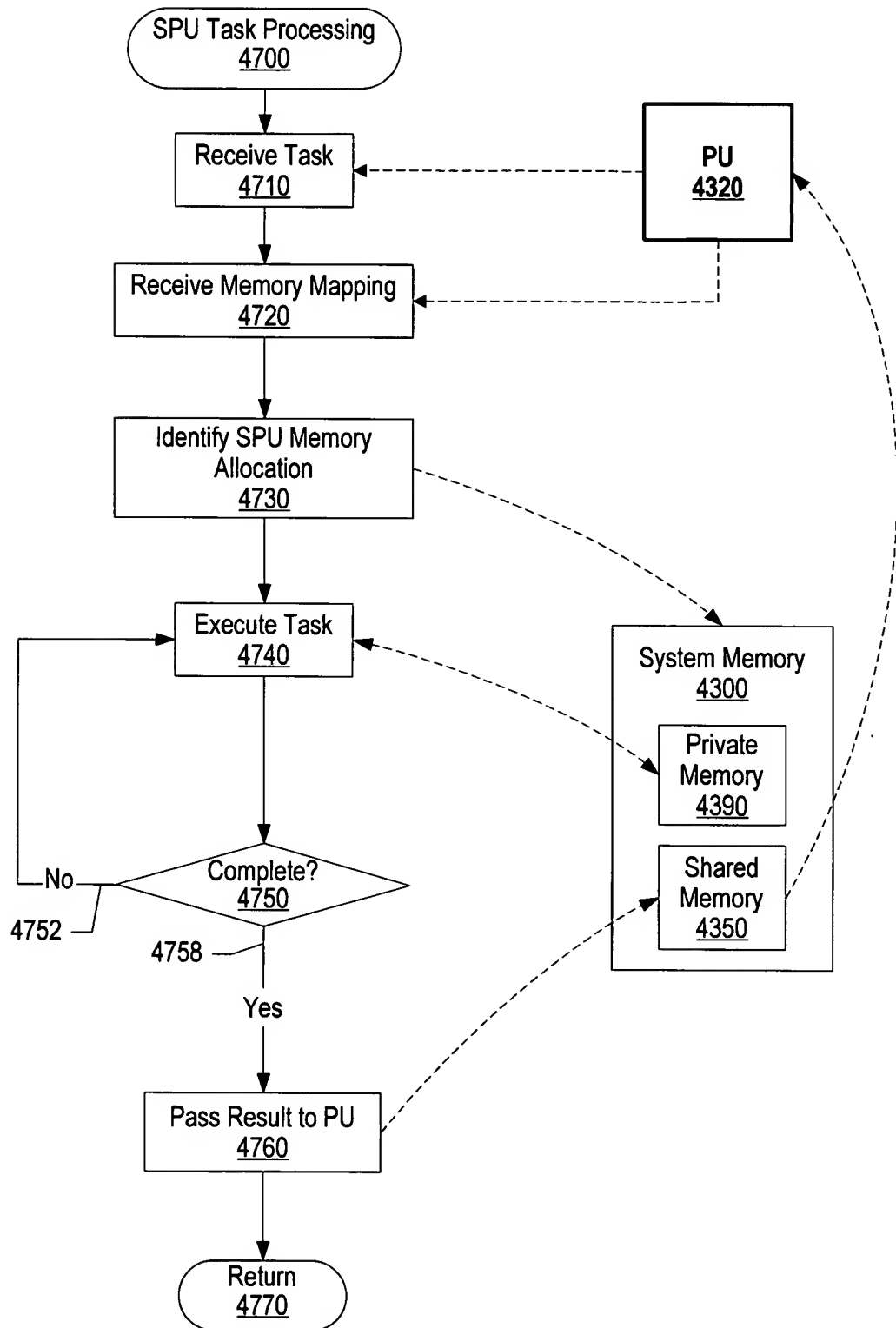


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